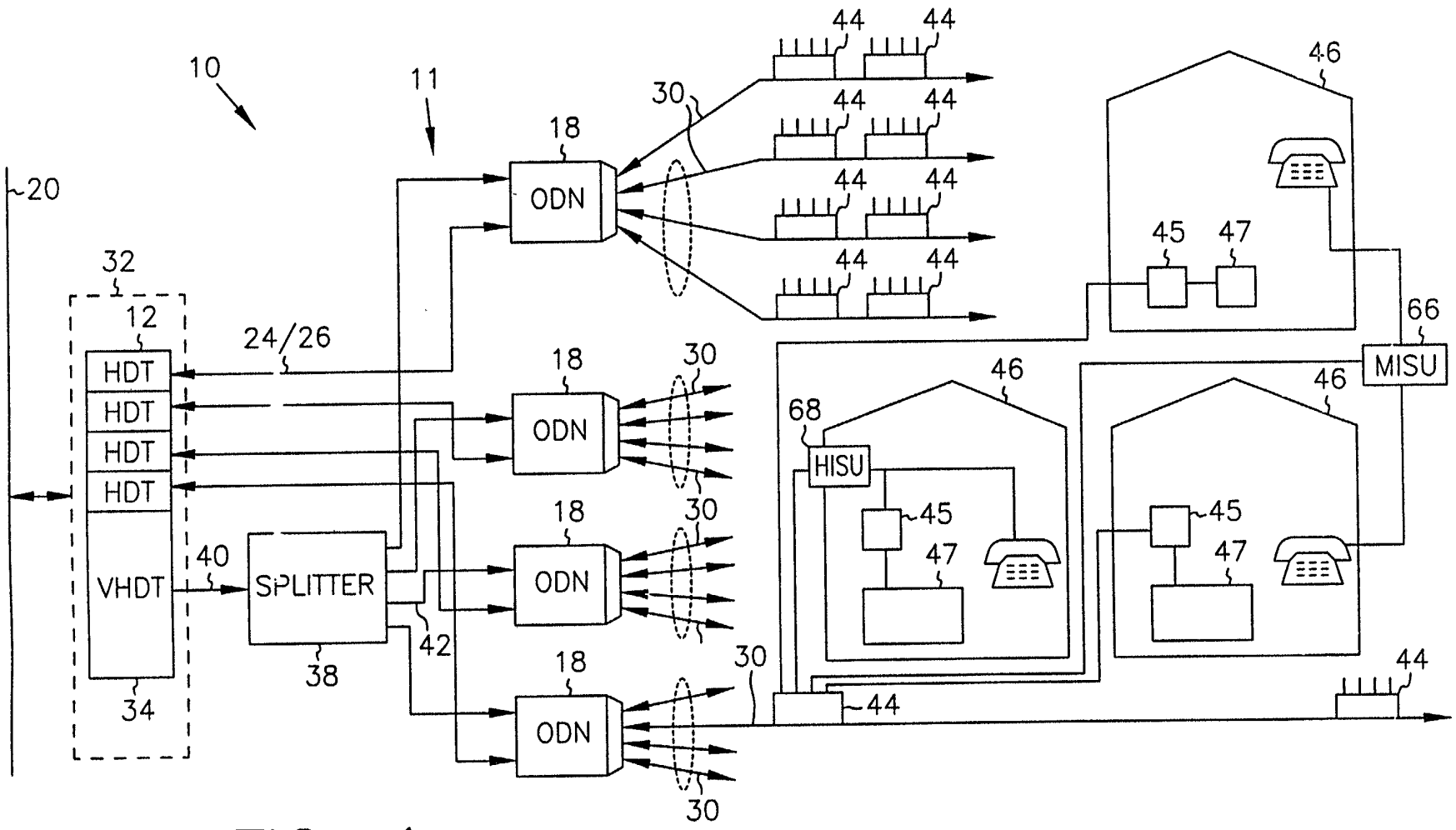


FIG. 1

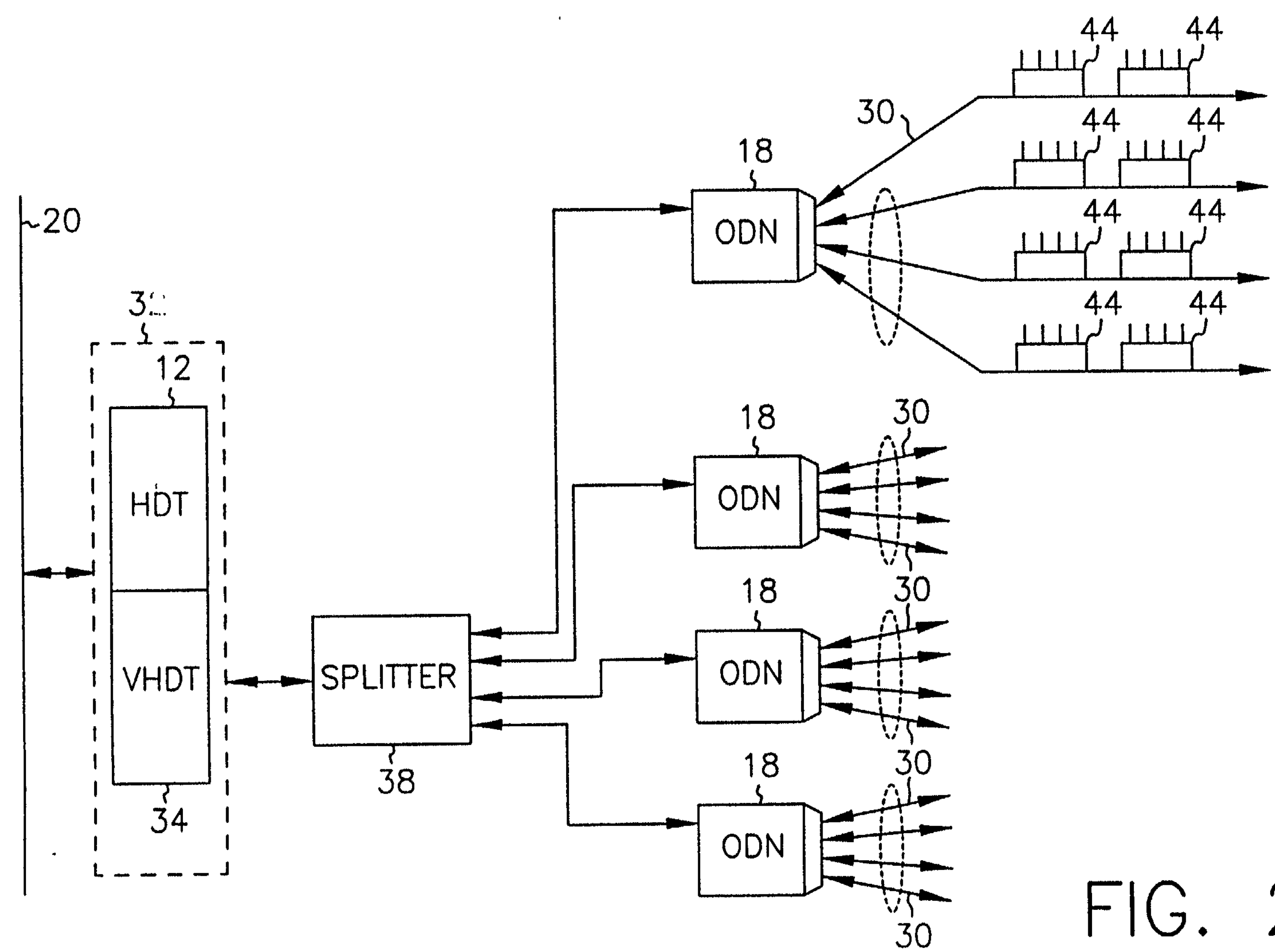


FIG. 2

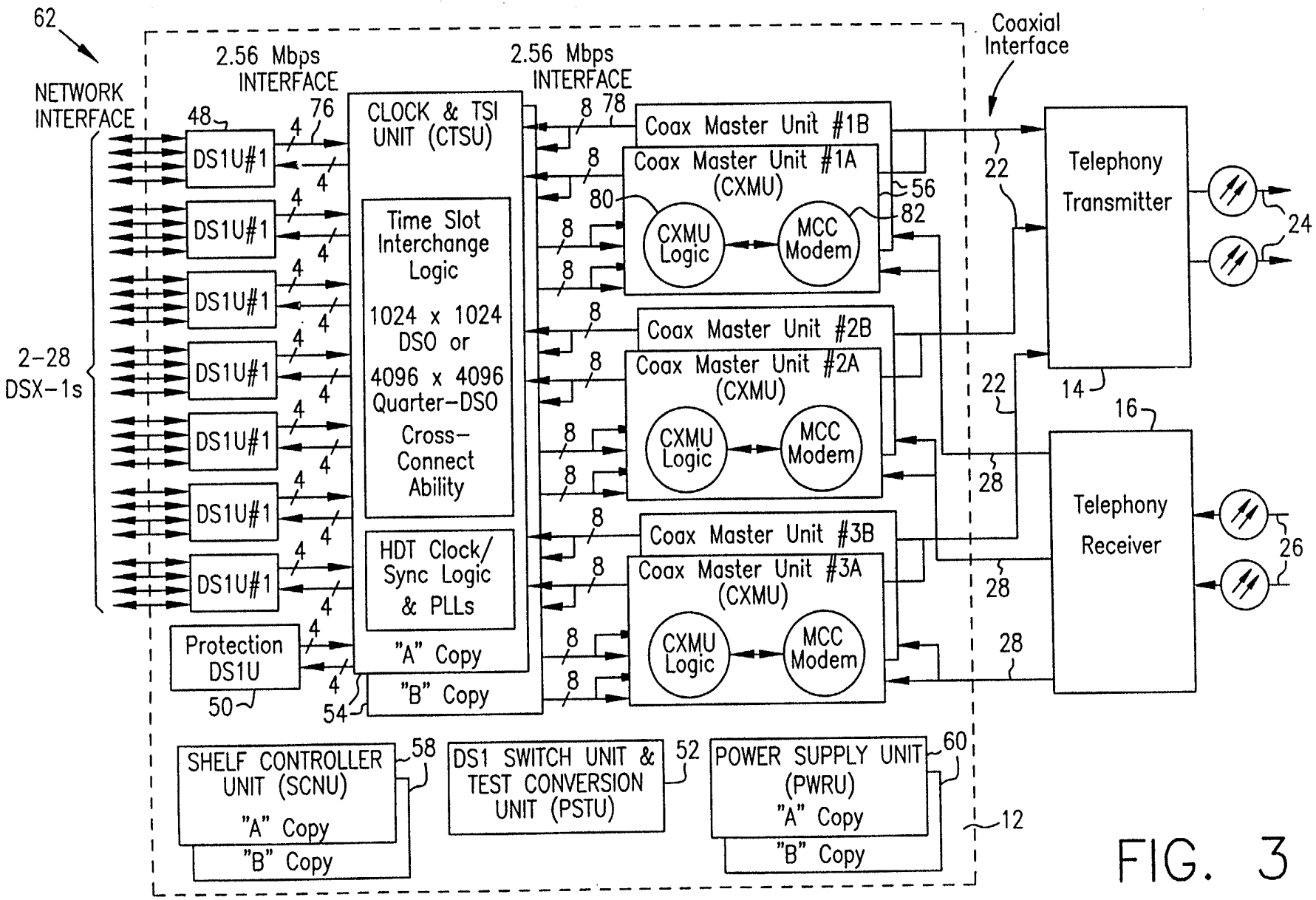
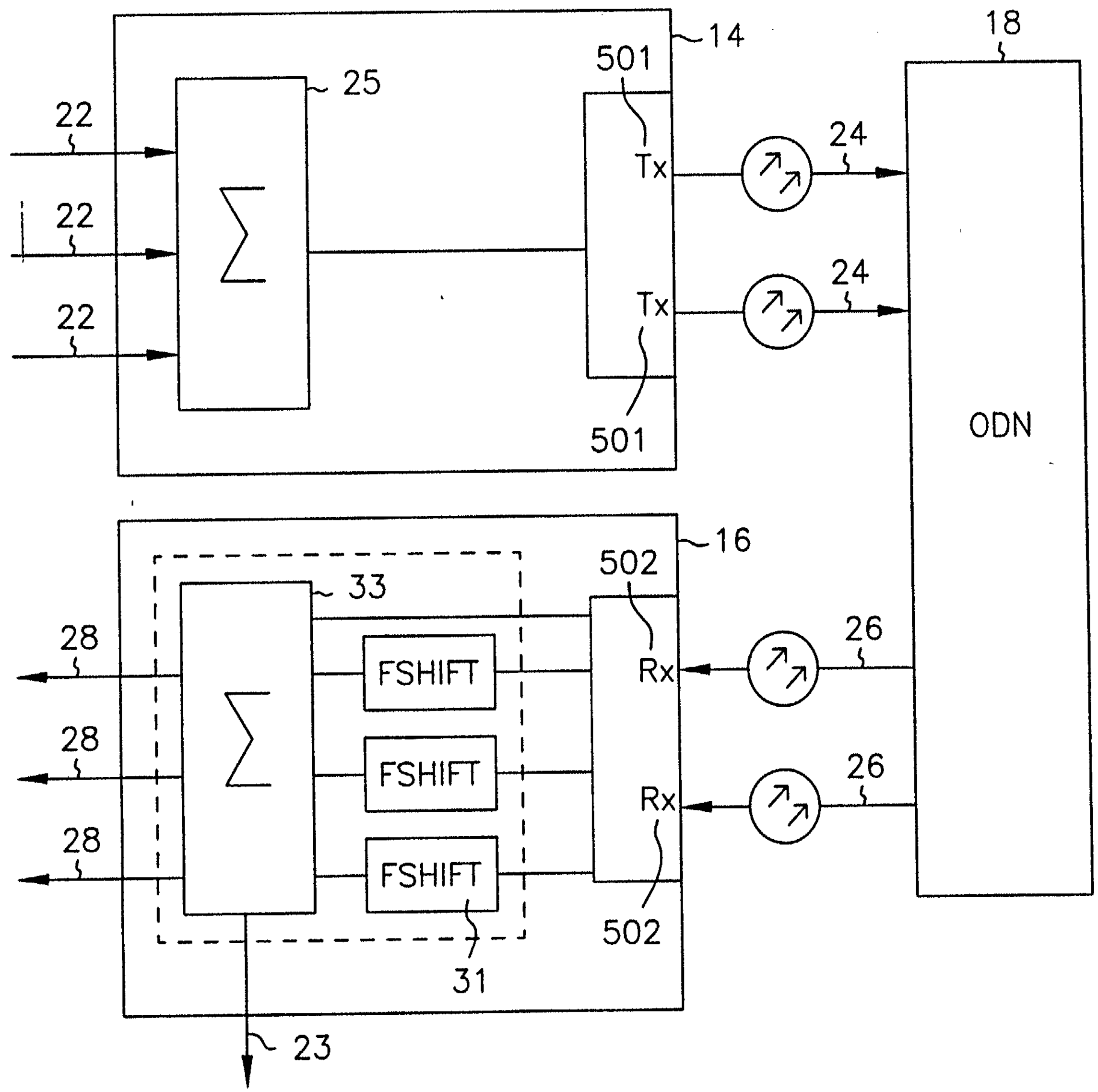

62
NETWORK INTERFACE
2-28 DSX-1s
2.56 Mbps INTERFACE
48
DS1U#1
DS1U#1
DS1U#1
DS1U#1
DS1U#1
DS1U#1
Protection DS1U
50
4
76
CLOCK & TSI UNIT (CTSU)
Time Slot Interchange Logic
1024 x 1024 DSO or
4096 x 4096 Quarter-DSO
Cross-Connect Ability
HDT Clock/ Sync Logic & PLLs
"A" Copy
"B" Copy
54
2.56 Mbps INTERFACE
8
78
Coax Master Unit #1B
Coax Master Unit #1A (CXMU)
80
CXMU Logic
MCC Modem
82
56
Coax Master Unit #2B
Coax Master Unit #2A (CXMU)
CXMU Logic
MCC Modem
Coax Master Unit #3B
Coax Master Unit #3A (CXMU)
CXMU Logic
MCC Modem
Coaxial Interface
22
28
Telephony Transmitter
14
16
Telephony Receiver
24
26
SHELF CONTROLLER UNIT (SCNU)
"A" Copy
"B" Copy
58
DS1 SWITCH UNIT & TEST CONVERSION UNIT (PSTU)
52
POWER SUPPLY UNIT (PWRU)
"A" Copy
"B" Copy
60
12

FIG. 3

FIG. 4



14
25
22
22
22
501
Tx
Tx
501
24
24
18
ODN
16
33
502
Rx
Rx
502
FSHIFT
FSHIFT
FSHIFT
31
26
26
28
28
28
23

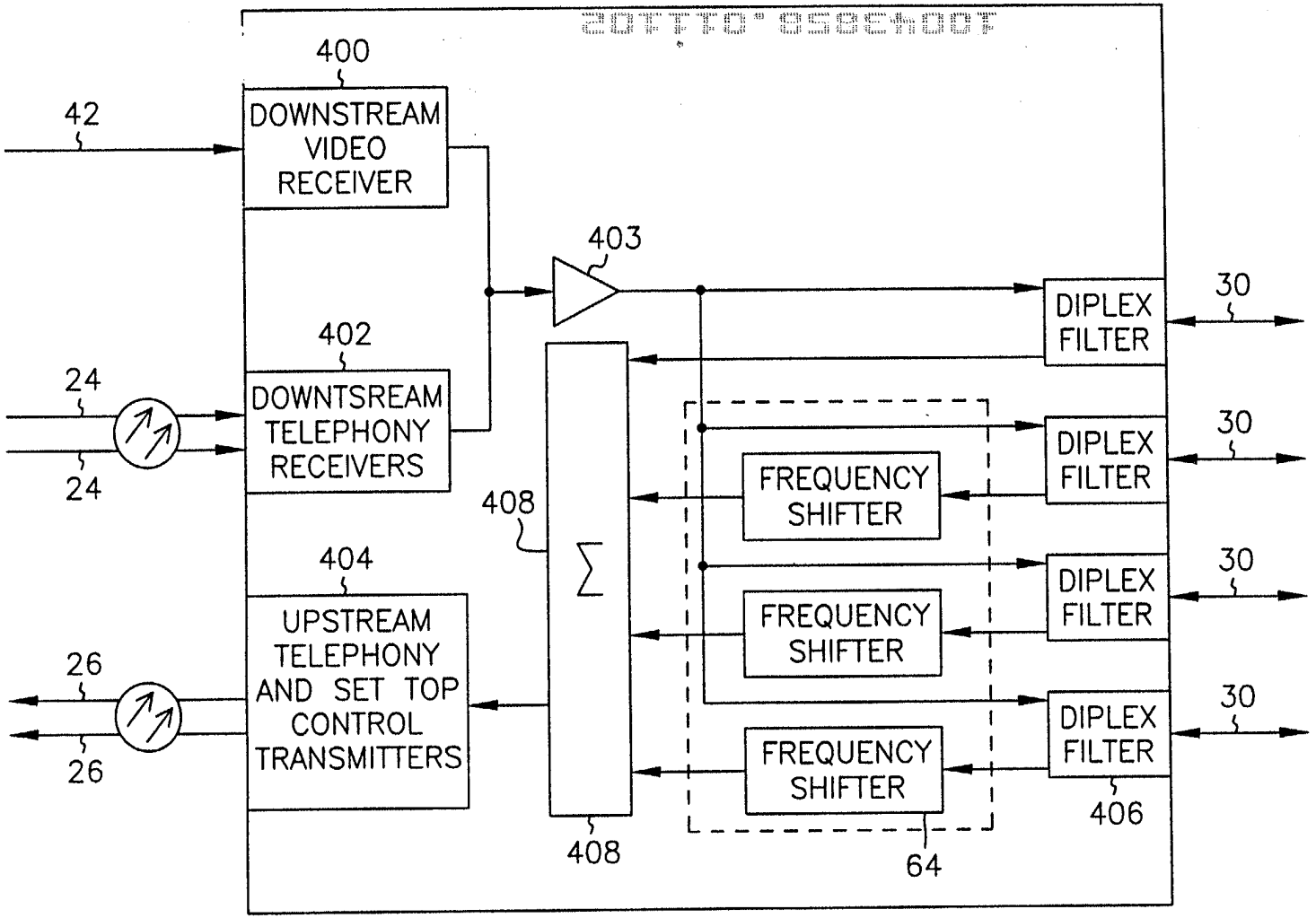

400
DOWNSTREAM VIDEO RECEIVER
42
403
402
DOWNTSREAM TELEPHONY RECEIVERS
24
24
408
404
UPSTREAM TELEPHONY AND SET TOP CONTROL TRANSMITTERS
26
26
DIPLEX FILTER
30
FREQUENCY SHIFTER
406
408
64

FIG. 5

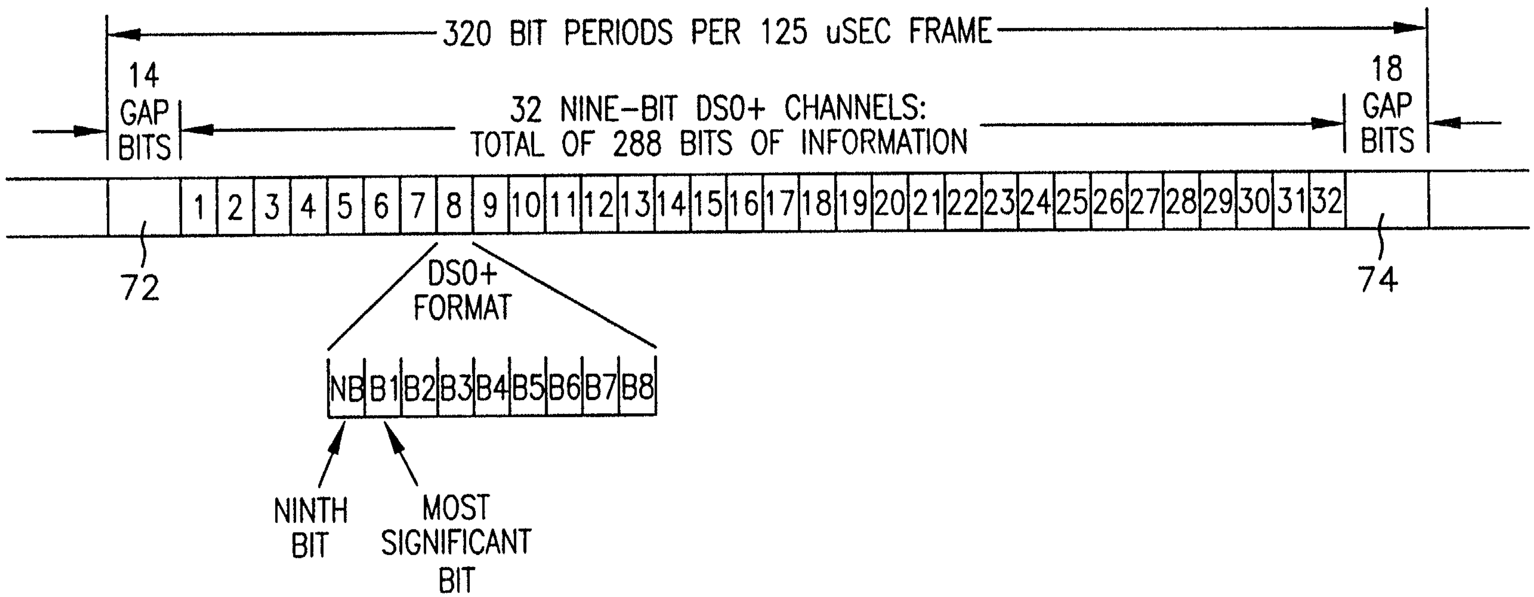

320 BIT PERIODS PER 125 uSEC FRAME
14 GAP BITS
32 NINE-BIT DS0+ CHANNELS:
TOTAL OF 288 BITS OF INFORMATION
18 GAP BITS
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
72
74
DS0+ FORMAT
NB B1 B2 B3 B4 B5 B6 B7 B8
NINTH BIT
MOST SIGNIFICANT BIT

FIG. 9

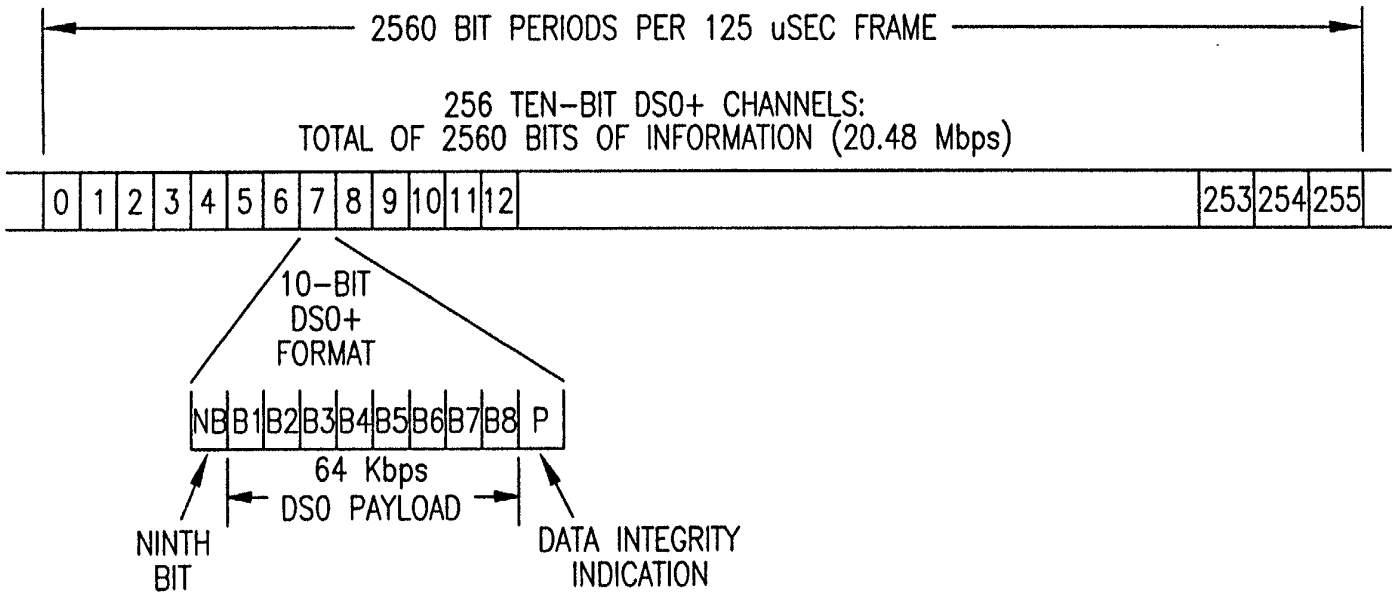

2560 BIT PERIODS PER 125 uSEC FRAME
256 TEN-BIT DS0+ CHANNELS:
TOTAL OF 2560 BITS OF INFORMATION (20.48 Mbps)
0 1 2 3 4 5 6 7 8 9 10 11 12
253 254 255
10-BIT
DS0+
FORMAT
NB B1 B2 B3 B4 B5 B6 B7 B8 P
64 Kbps
DS0 PAYLOAD
NINTH
BIT
DATA INTEGRITY
INDICATION

FIG. 10

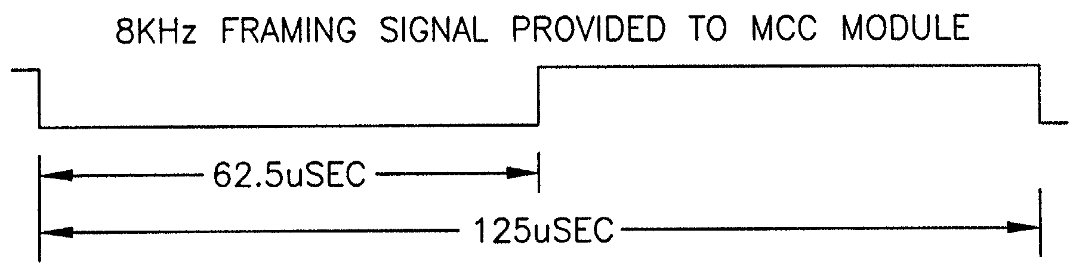

8KHz FRAMING SIGNAL PROVIDED TO MCC MODULE
62.5uSEC
125uSEC

FIG. 11

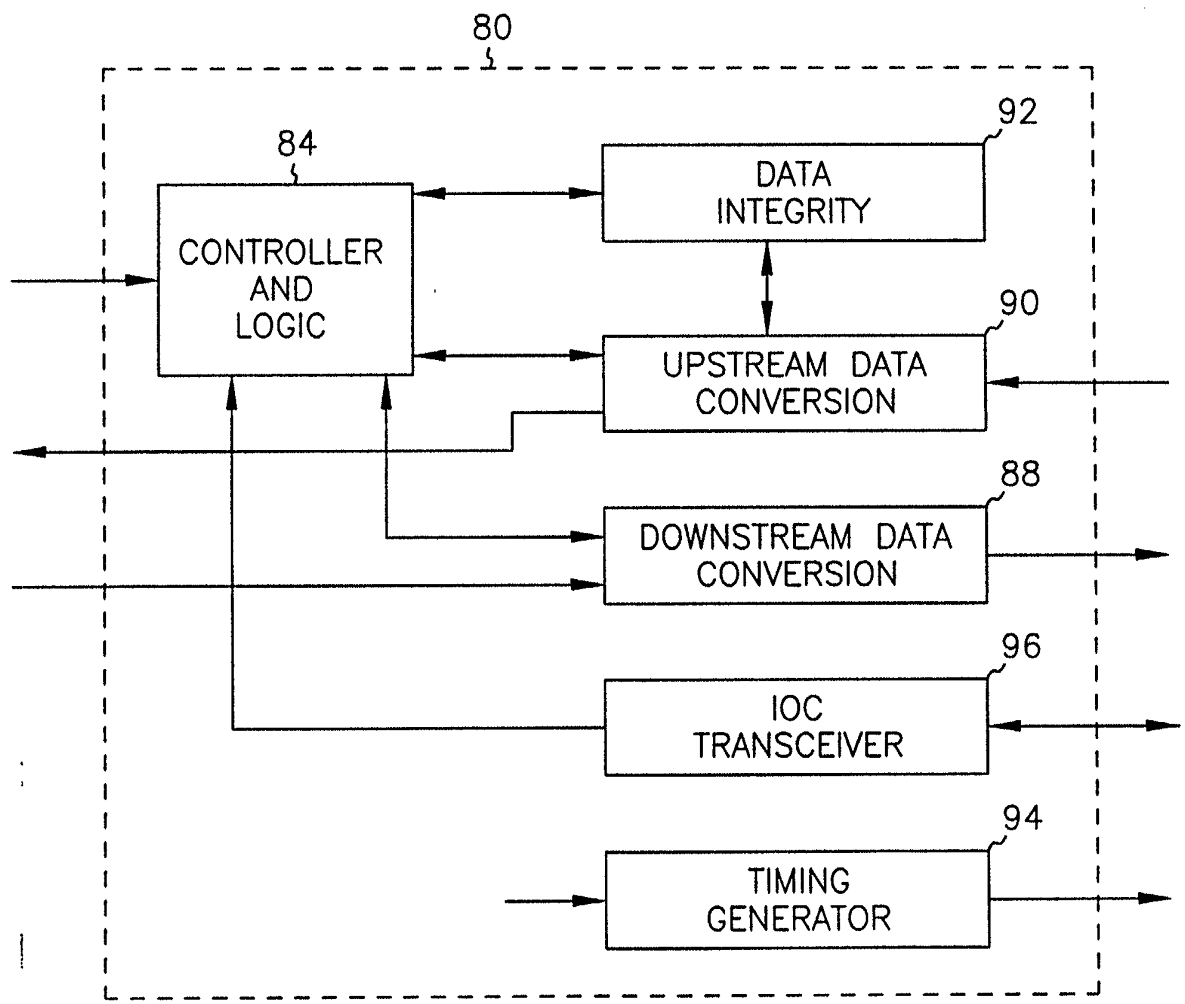

80
84
CONTROLLER
AND
LOGIC
92
DATA
INTEGRITY
90
UPSTREAM DATA
CONVERSION
88
DOWNSTREAM DATA
CONVERSION
96
IOC
TRANSCEIVER
94
TIMING
GENERATOR

FIG. 12

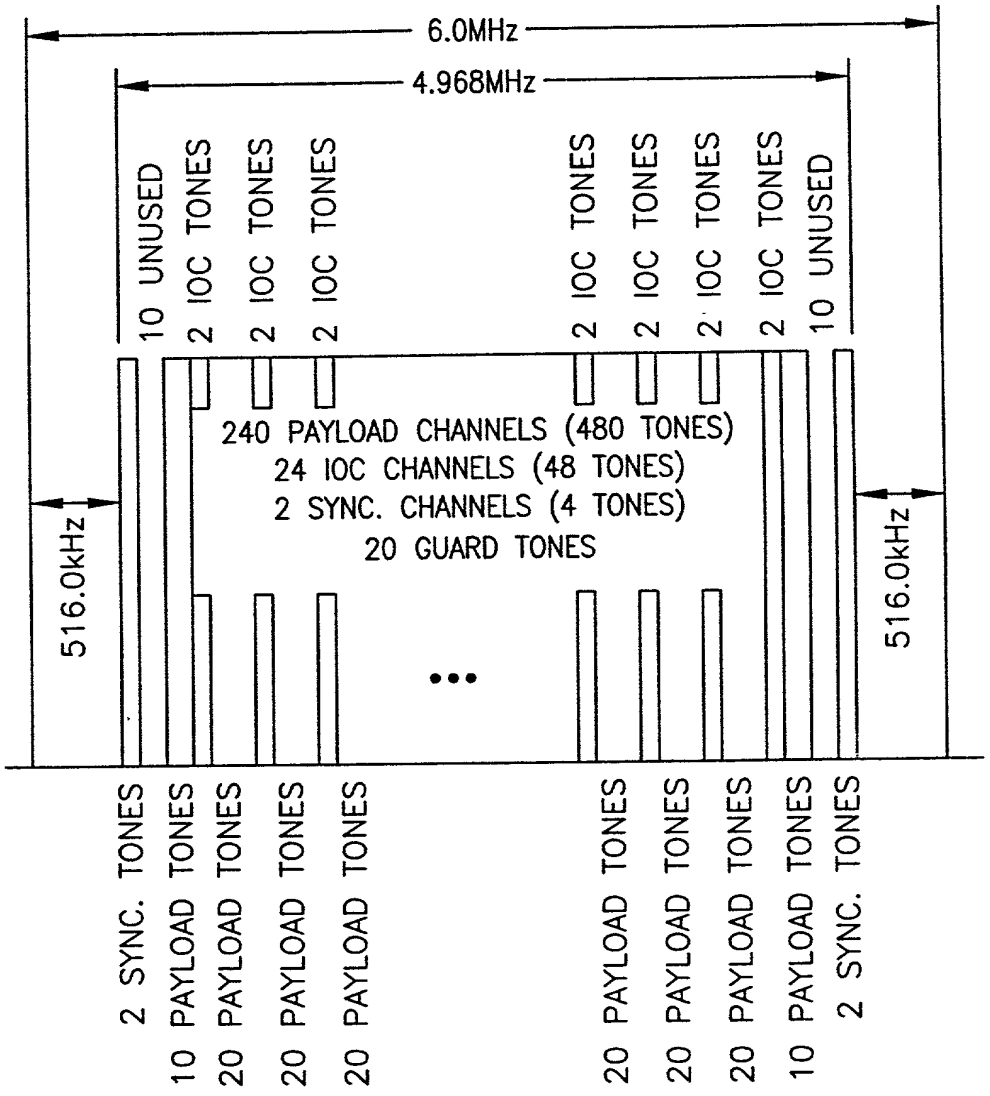

6.0MHz
4.968MHz
10 UNUSED
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
10 UNUSED
240 PAYLOAD CHANNELS (480 TONES)
24 IOC CHANNELS (48 TONES)
2 SYNC. CHANNELS (4 TONES)
20 GUARD TONES
516.0kHz
516.0kHz
2 SYNC. TONES
10 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
10 PAYLOAD TONES
2 SYNC. TONES

FIG. 13

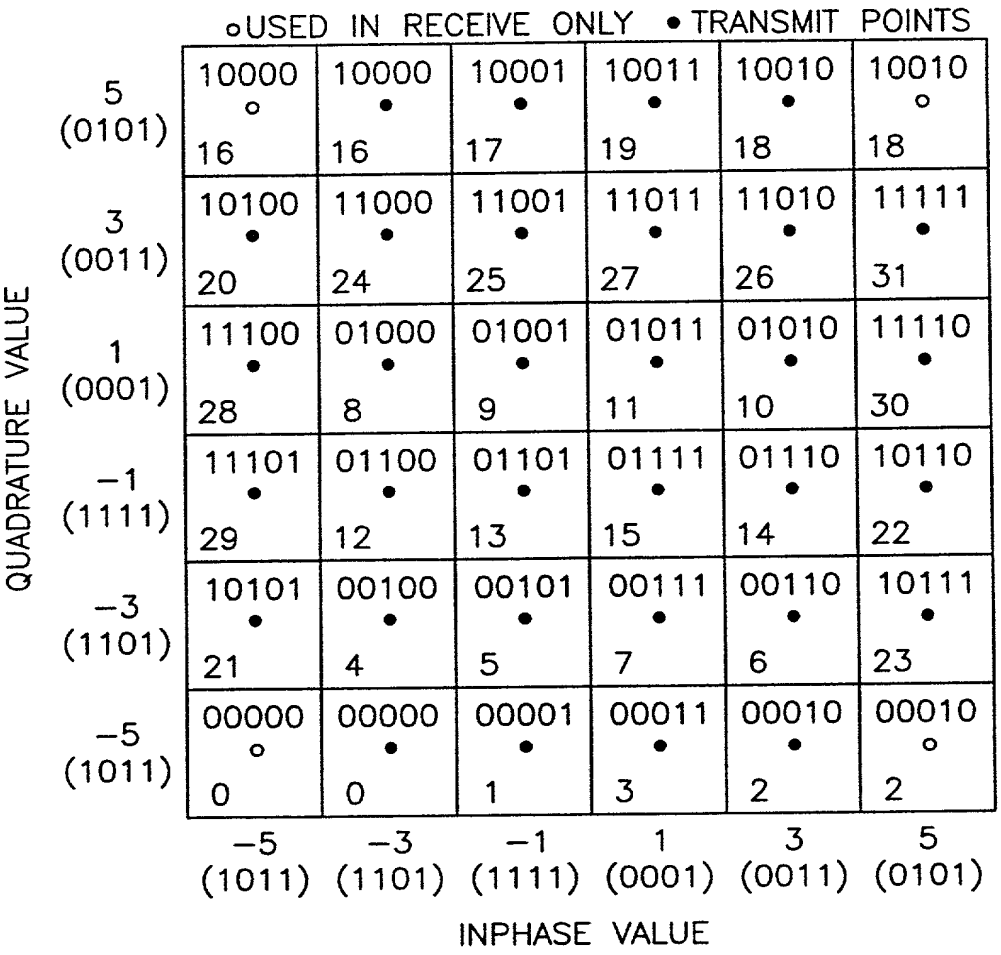


FIG. 14

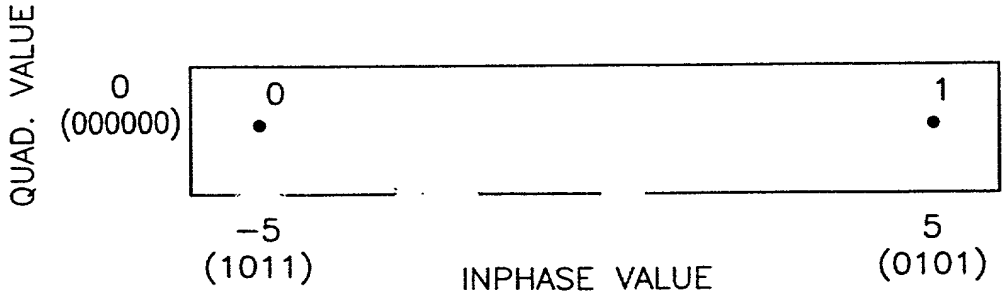


FIG. 15

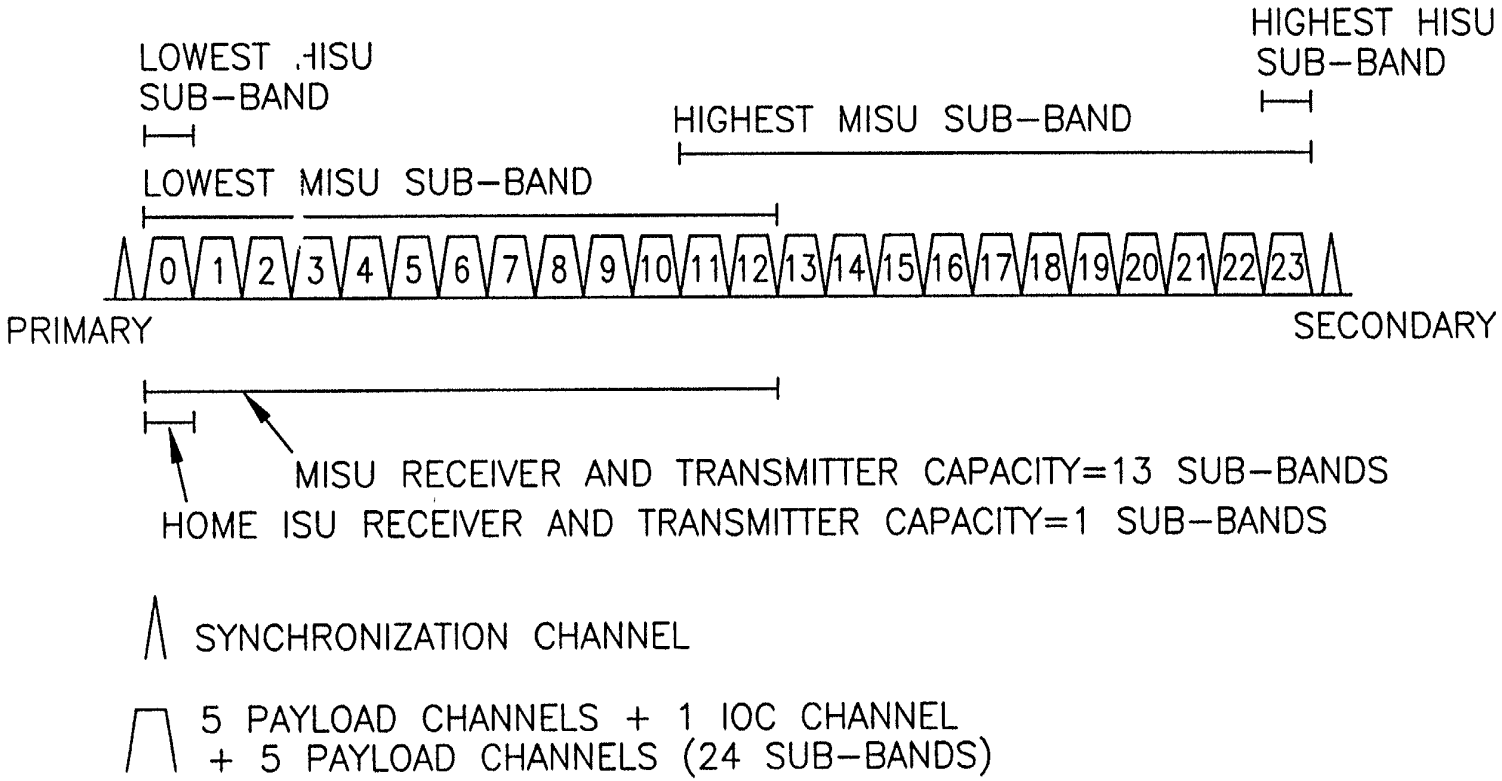

HIGHEST HISU
SUB-BAND
LOWEST HISU
SUB-BAND
HIGHEST MISU SUB-BAND
LOWEST MISU SUB-BAND
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
PRIMARY
SECONDARY
MISU RECEIVER AND TRANSMITTER CAPACITY=13 SUB-BANDS
HOME ISU RECEIVER AND TRANSMITTER CAPACITY=1 SUB-BANDS
SYNCHRONIZATION CHANNEL
5 PAYLOAD CHANNELS + 1 IOC CHANNEL
+ 5 PAYLOAD CHANNELS (24 SUB-BANDS)

FIG. 16

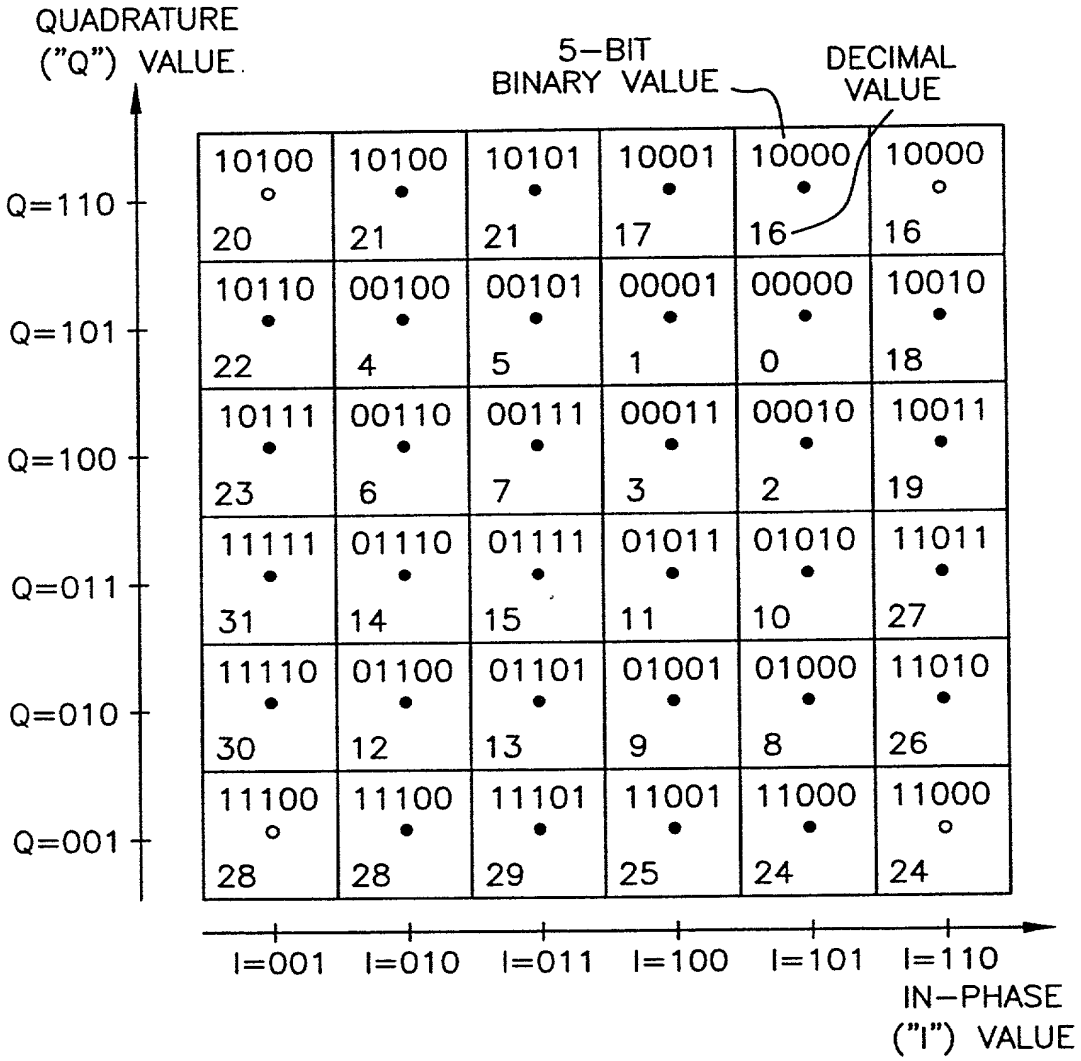

QUADRATURE ("Q") VALUE
5-BIT BINARY VALUE
DECIMAL VALUE
Q=110
Q=101
Q=100
Q=011
Q=010
Q=001
10100 20
10100 21
10101 21
10001 17
10000 16
10000 16
10110 22
00100 4
00101 5
00001 1
00000 0
10010 18
10111 23
00110 6
00111 7
00011 3
00010 2
10011 19
11111 31
01110 14
01111 15
01011 11
01010 10
11011 27
11110 30
01100 12
01101 13
01001 9
01000 8
11010 26
11100 28
11100 28
11101 29
11001 25
11000 24
11000 24
I=001
I=010
I=011
I=100
I=101
I=110
IN-PHASE ("I") VALUE

FIG. 17

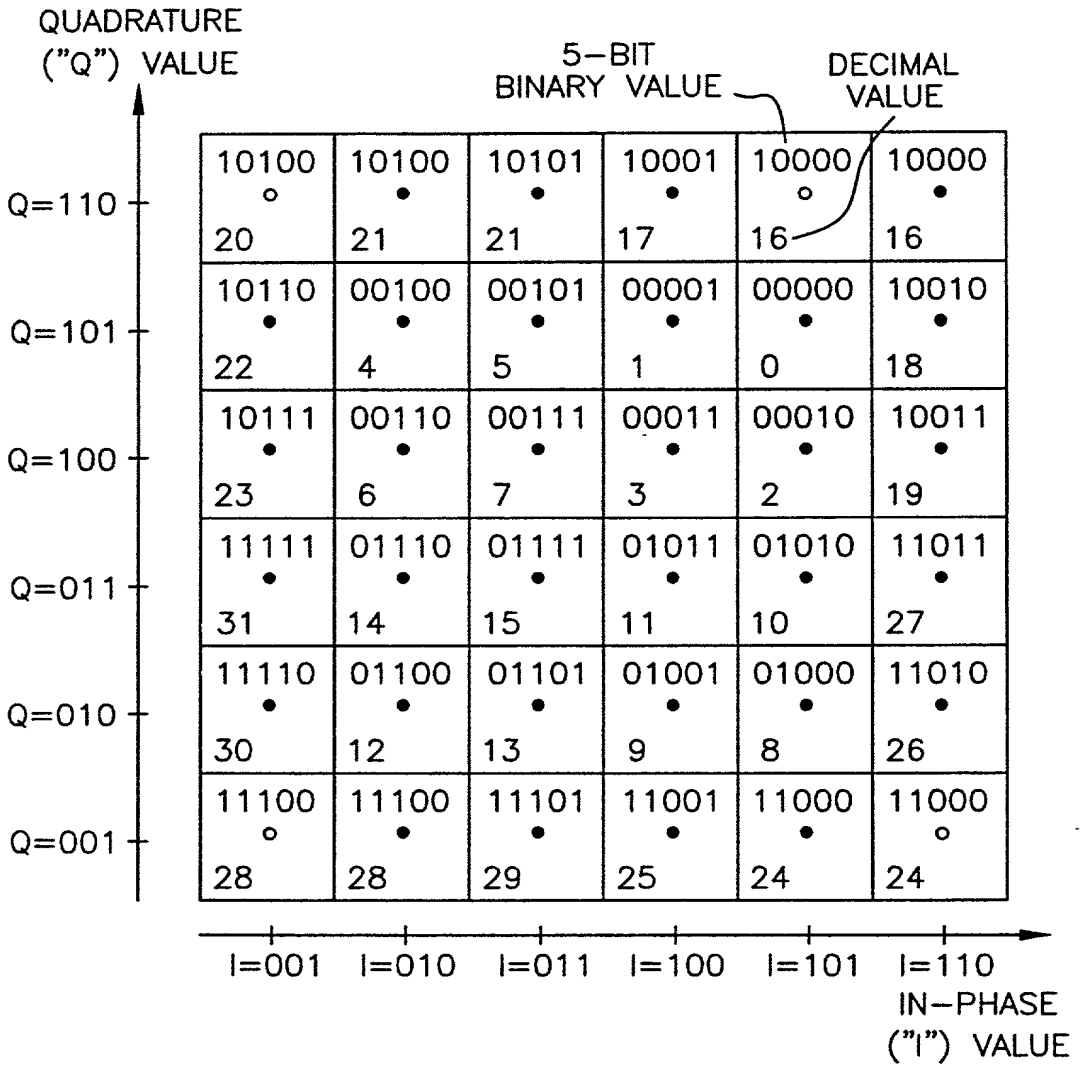

QUADRATURE
("Q") VALUE
5-BIT
BINARY VALUE
DECIMAL
VALUE
Q=110
Q=101
Q=100
Q=011
Q=010
Q=001
10100 20
10100 21
10101 21
10001 17
10000 16
10000 16
10110 22
00100 4
00101 5
00001 1
00000 0
10010 18
10111 23
00110 6
00111 7
00011 3
00010 2
10011 19
11111 31
01110 14
01111 15
01011 11
01010 10
11011 27
11110 30
01100 12
01101 13
01001 9
01000 8
11010 26
11100 28
11100 28
11101 29
11001 25
11000 24
11000 24
I=001
I=010
I=011
I=100
I=101
I=110
IN-PHASE
("I") VALUE

FIG. 18

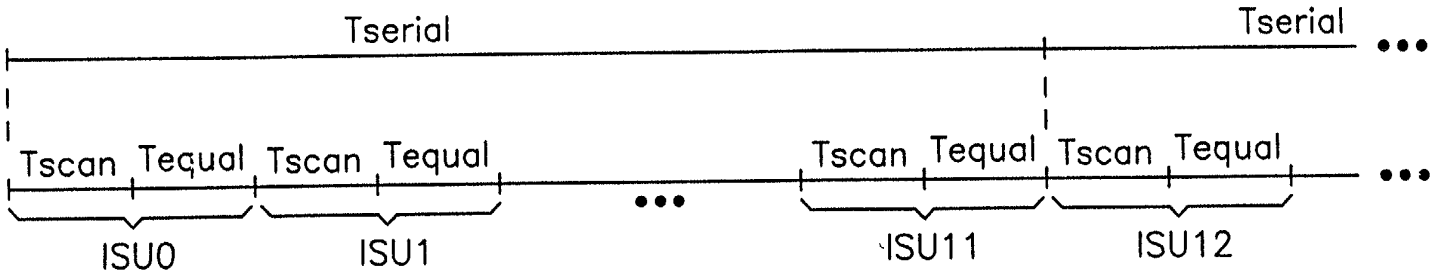

Tserial
Tserial
Tscan
Tequal
Tscan
Tequal
Tscan
Tequal
Tscan
Tequal
ISU0
ISU1
ISU11
ISU12

FIG. 19

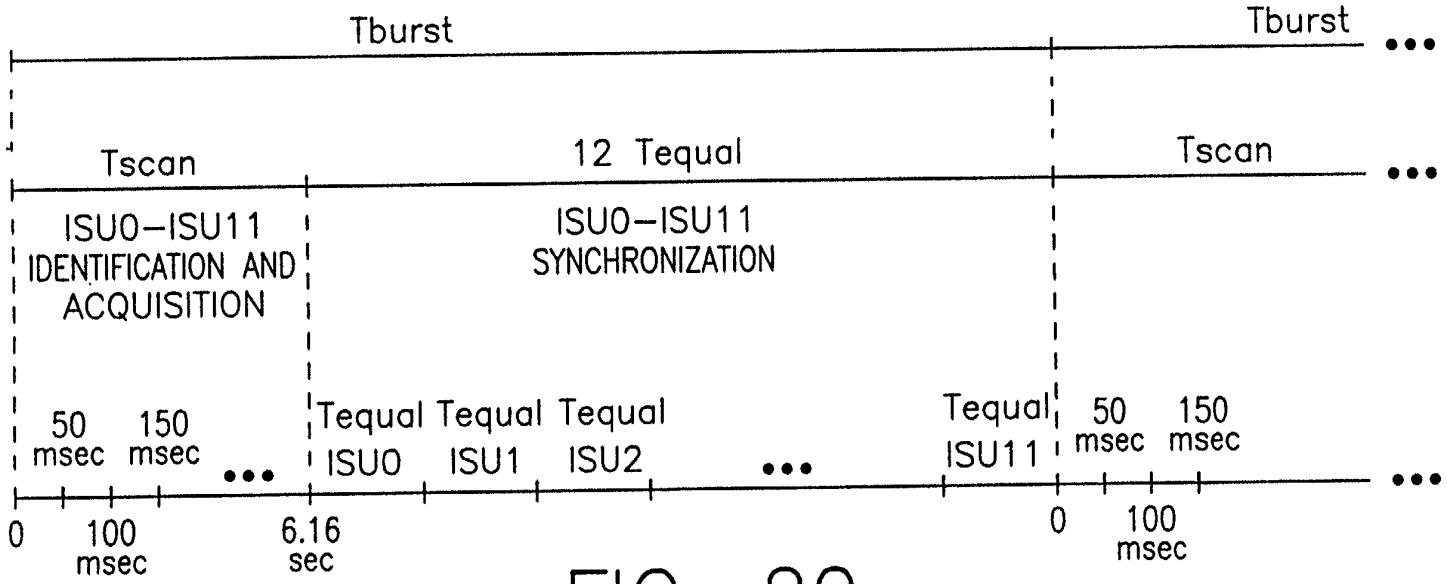

Tburst
Tburst
Tscan
12 Tequal
Tscan
ISU0–ISU11
IDENTIFICATION AND
ACQUISITION
ISU0–ISU11
SYNCHRONIZATION
50
msec
150
msec
Tequal
ISU0
Tequal
ISU1
Tequal
ISU2
Tequal
ISU11
50
msec
150
msec
0
100
msec
6.16
sec
0
100
msec

FIG. 20

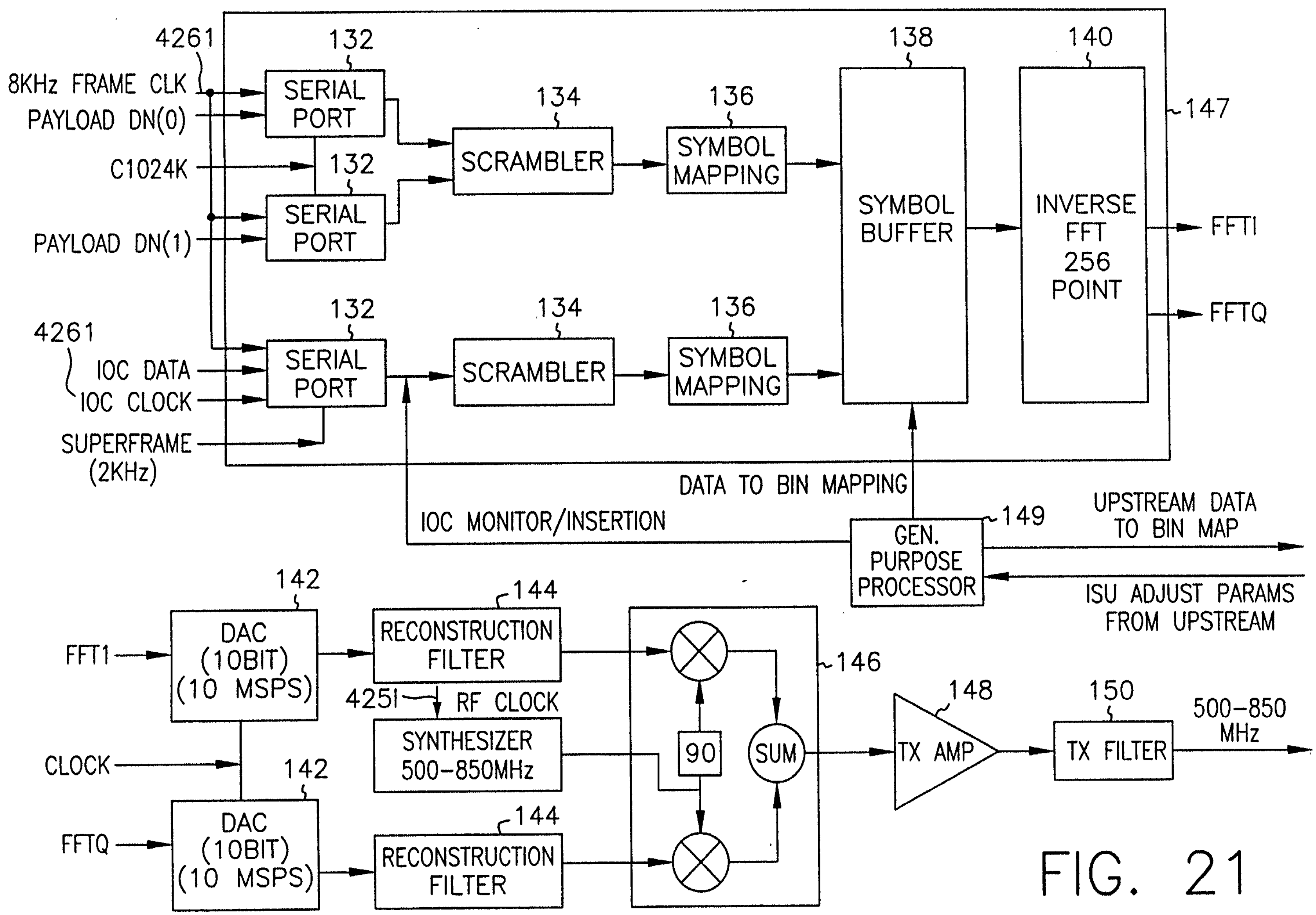

4261
8KHz FRAME CLK
PAYLOAD DN(0)
C1024K
PAYLOAD DN(1)
4261
IOC DATA
IOC CLOCK
SUPERFRAME (2KHz)
132
SERIAL PORT
132
SERIAL PORT
132
SERIAL PORT
134
SCRAMBLER
134
SCRAMBLER
136
SYMBOL MAPPING
136
SYMBOL MAPPING
138
SYMBOL BUFFER
140
INVERSE FFT 256 POINT
147
FFTI
FFTQ
DATA TO BIN MAPPING
IOC MONITOR/INSERTION
149
GEN. PURPOSE PROCESSOR
UPSTREAM DATA TO BIN MAP
ISU ADJUST PARAMS FROM UPSTREAM
FFT1
CLOCK
FFTQ
142
DAC (10BIT) (10 MSPS)
142
DAC (10BIT) (10 MSPS)
144
RECONSTRUCTION FILTER
144
RECONSTRUCTION FILTER
4251
RF CLOCK
SYNTHESIZER 500-850MHz
146
90
SUM
148
TX AMP
150
TX FILTER
500-850 MHz

FIG. 21

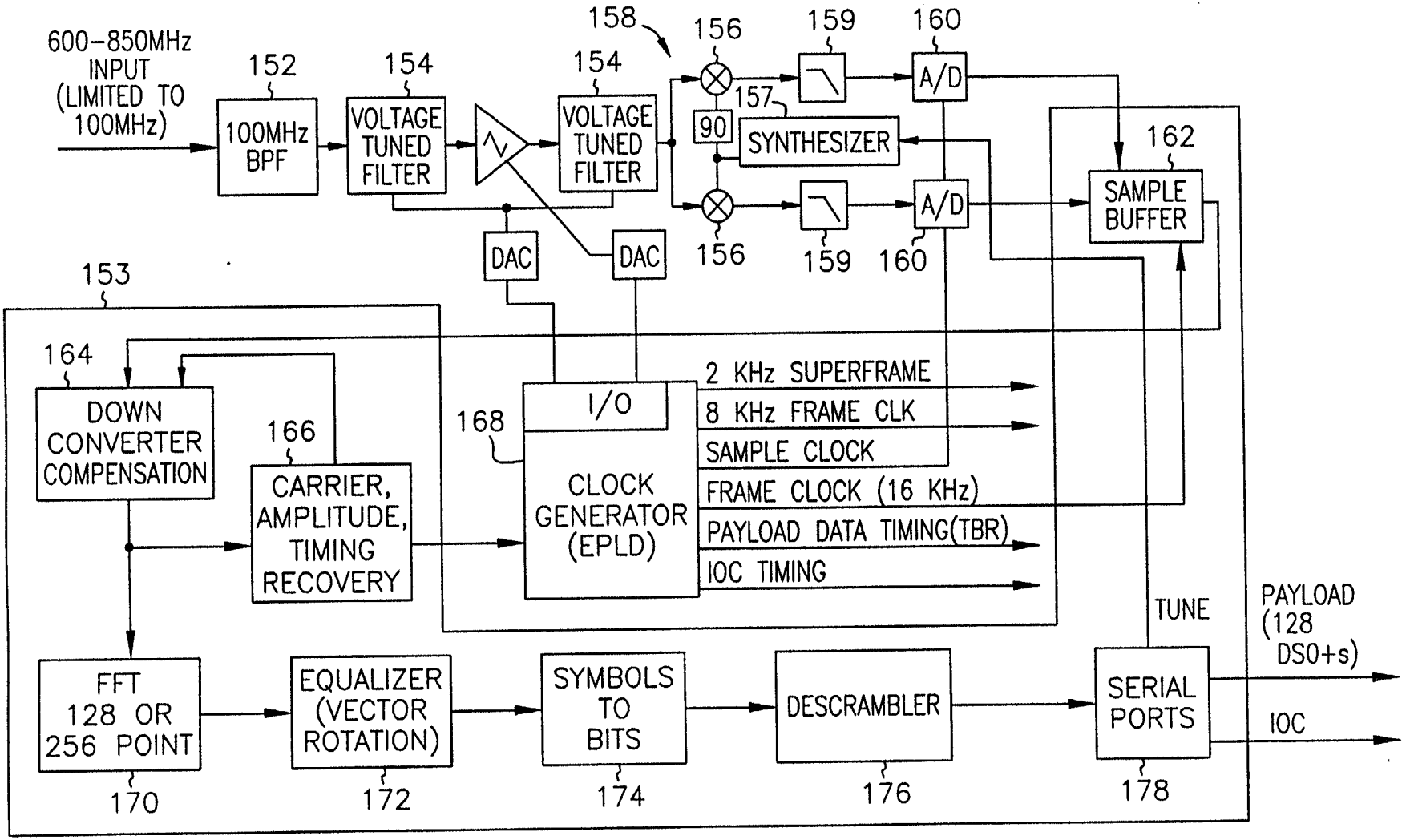

600–850MHz INPUT (LIMITED TO 100MHz)
152
100MHz BPF
154
VOLTAGE TUNED FILTER
154
VOLTAGE TUNED FILTER
158
156
159
160
A/D
157
90
SYNTHESIZER
162
SAMPLE BUFFER
156
159
160
A/D
DAC
DAC
153
164
DOWN CONVERTER COMPENSATION
166
CARRIER, AMPLITUDE, TIMING RECOVERY
168
I/O
CLOCK GENERATOR (EPLD)
2 KHz SUPERFRAME
8 KHz FRAME CLK
SAMPLE CLOCK
FRAME CLOCK (16 KHz)
PAYLOAD DATA TIMING(TBR)
IOC TIMING
TUNE
PAYLOAD (128 DS0+s)
IOC
FFT 128 OR 256 POINT
170
EQUALIZER (VECTOR ROTATION)
172
SYMBOLS TO BITS
174
DESCRAMBLER
176
SERIAL PORTS
178

FIG. 22

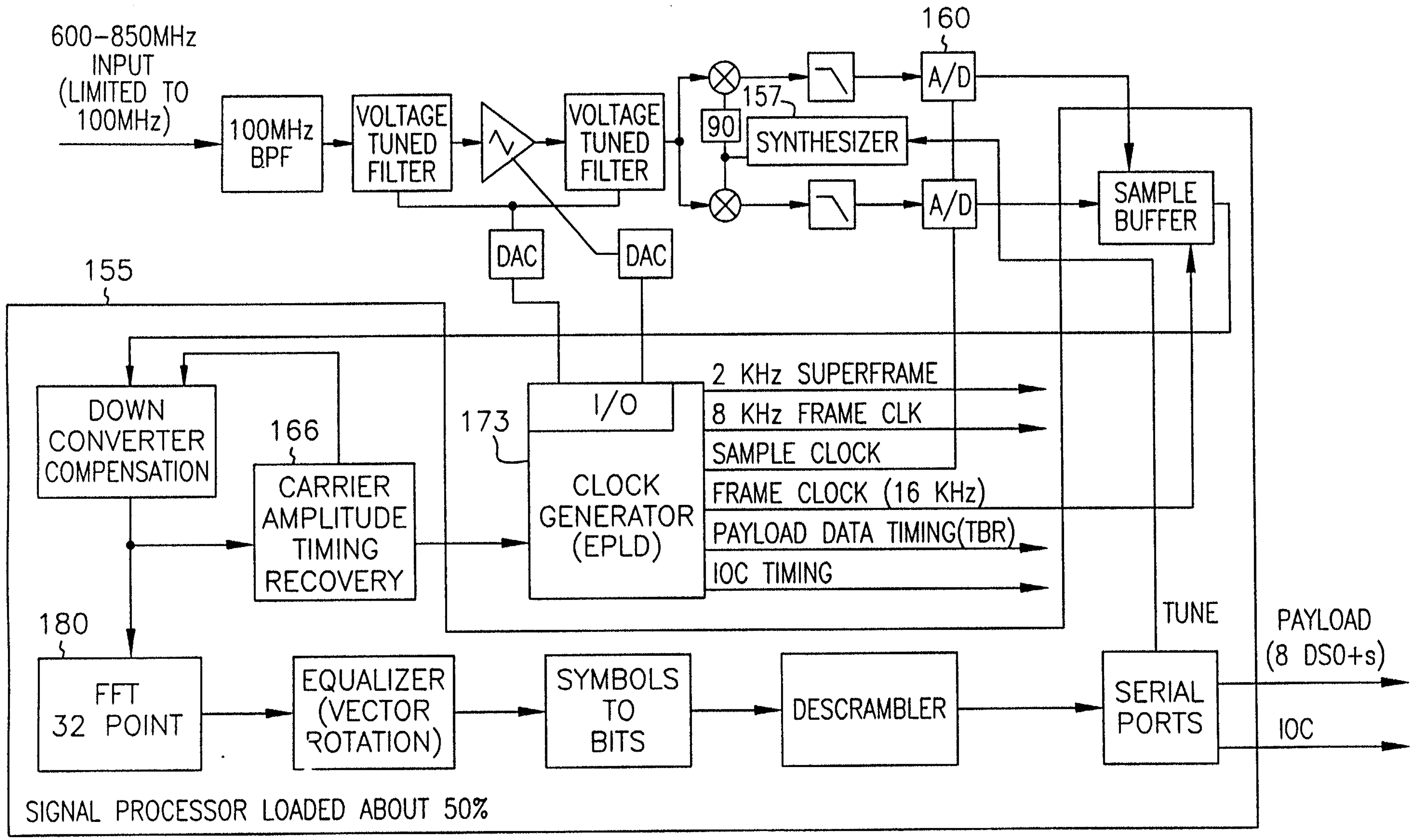

600–850MHz INPUT (LIMITED TO 100MHz)
100MHz BPF
VOLTAGE TUNED FILTER
VOLTAGE TUNED FILTER
DAC
DAC
90
157
SYNTHESIZER
160
A/D
A/D
SAMPLE BUFFER
155
DOWN CONVERTER COMPENSATION
166
CARRIER AMPLITUDE TIMING RECOVERY
173
I/O
CLOCK GENERATOR (EPLD)
2 KHz SUPERFRAME
8 KHz FRAME CLK
SAMPLE CLOCK
FRAME CLOCK (16 KHz)
PAYLOAD DATA TIMING(TBR)
IOC TIMING
TUNE
PAYLOAD (8 DS0+s)
IOC
180
FFT 32 POINT
EQUALIZER (VECTOR ROTATION)
SYMBOLS TO BITS
DESCRAMBLER
SERIAL PORTS
SIGNAL PROCESSOR LOADED ABOUT 50%

FIG. 23

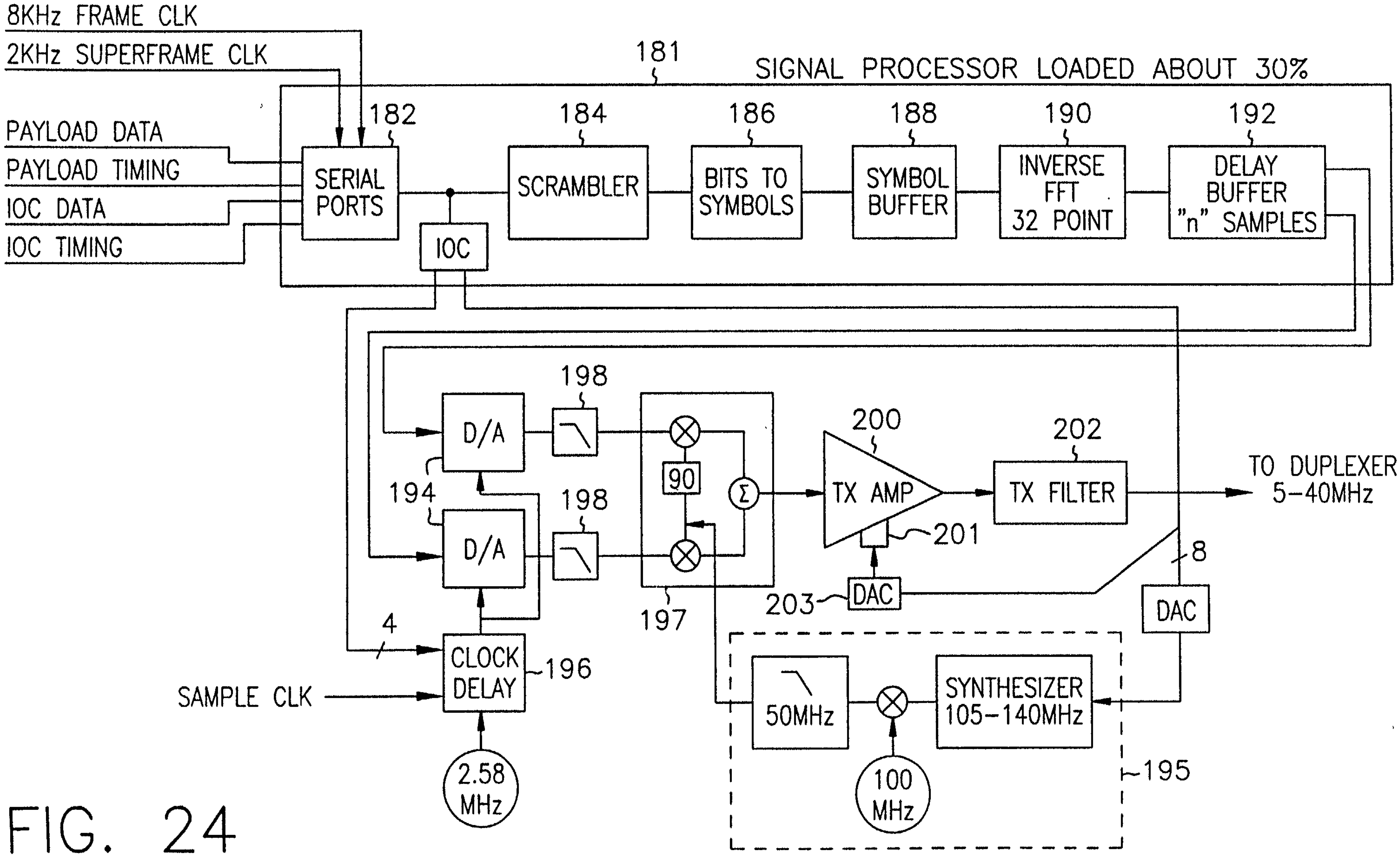

8KHz FRAME CLK
2KHz SUPERFRAME CLK
PAYLOAD DATA
PAYLOAD TIMING
IOC DATA
IOC TIMING
181
SIGNAL PROCESSOR LOADED ABOUT 30%
182
SERIAL PORTS
184
SCRAMBLER
186
BITS TO SYMBOLS
188
SYMBOL BUFFER
190
INVERSE FFT 32 POINT
192
DELAY BUFFER "n" SAMPLES
IOC
198
D/A
194
D/A
198
90
Σ
197
200
TX AMP
201
202
TX FILTER
TO DUPLEXER 5-40MHz
8
DAC
203
DAC
4
CLOCK DELAY
196
SAMPLE CLK
2.58 MHz
50MHz
SYNTHESIZER 105-140MHz
100 MHz
195

FIG. 24

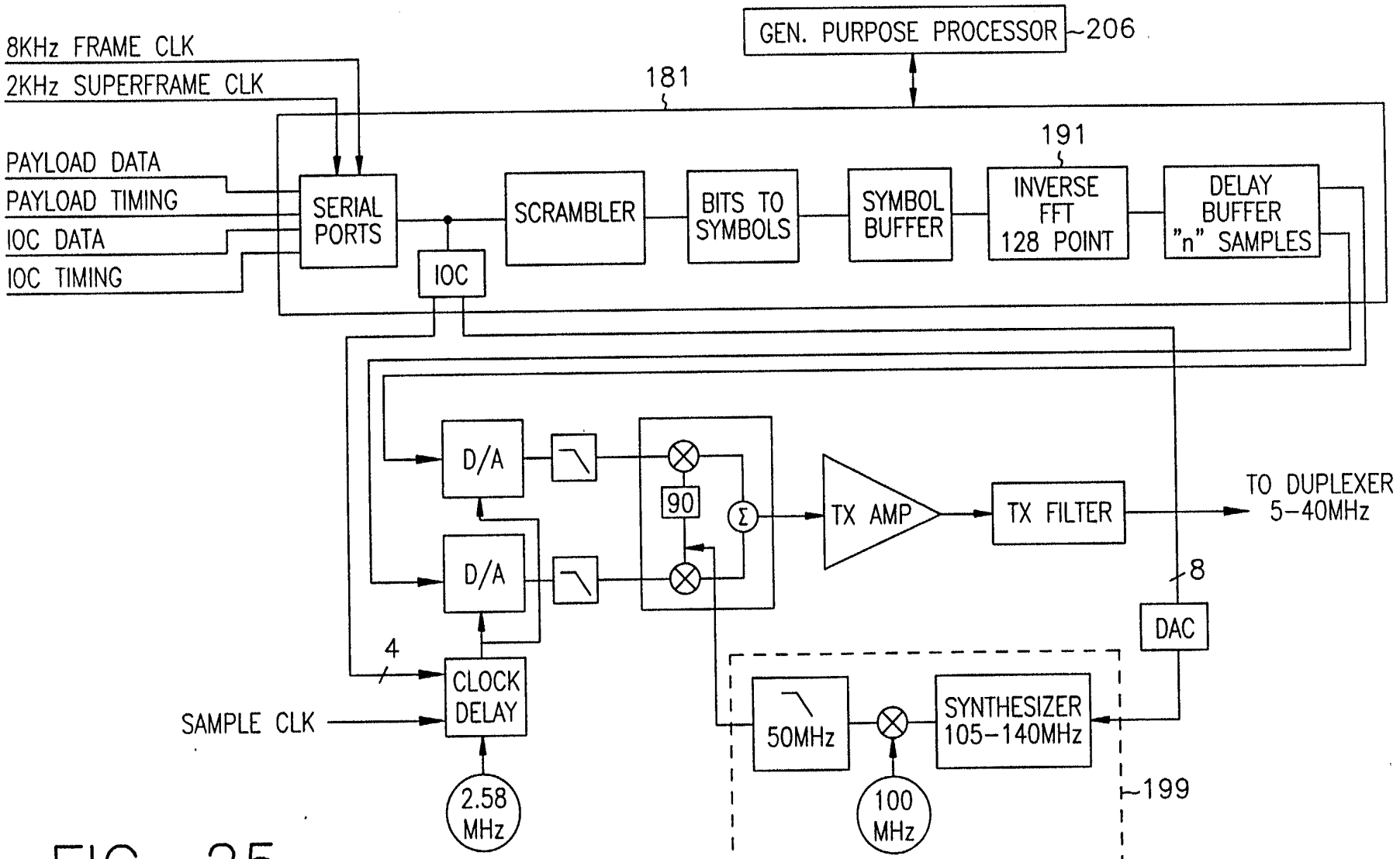

GEN. PURPOSE PROCESSOR
206
181
191
8KHz FRAME CLK
2KHz SUPERFRAME CLK
PAYLOAD DATA
PAYLOAD TIMING
IOC DATA
IOC TIMING
SERIAL PORTS
IOC
SCRAMBLER
BITS TO SYMBOLS
SYMBOL BUFFER
INVERSE FFT 128 POINT
DELAY BUFFER "n" SAMPLES
D/A
D/A
90
Σ
TX AMP
TX FILTER
TO DUPLEXER 5-40MHz
8
DAC
4
CLOCK DELAY
SAMPLE CLK
2.58 MHz
50MHz
100 MHz
SYNTHESIZER 105-140MHz
199

FIG. 25

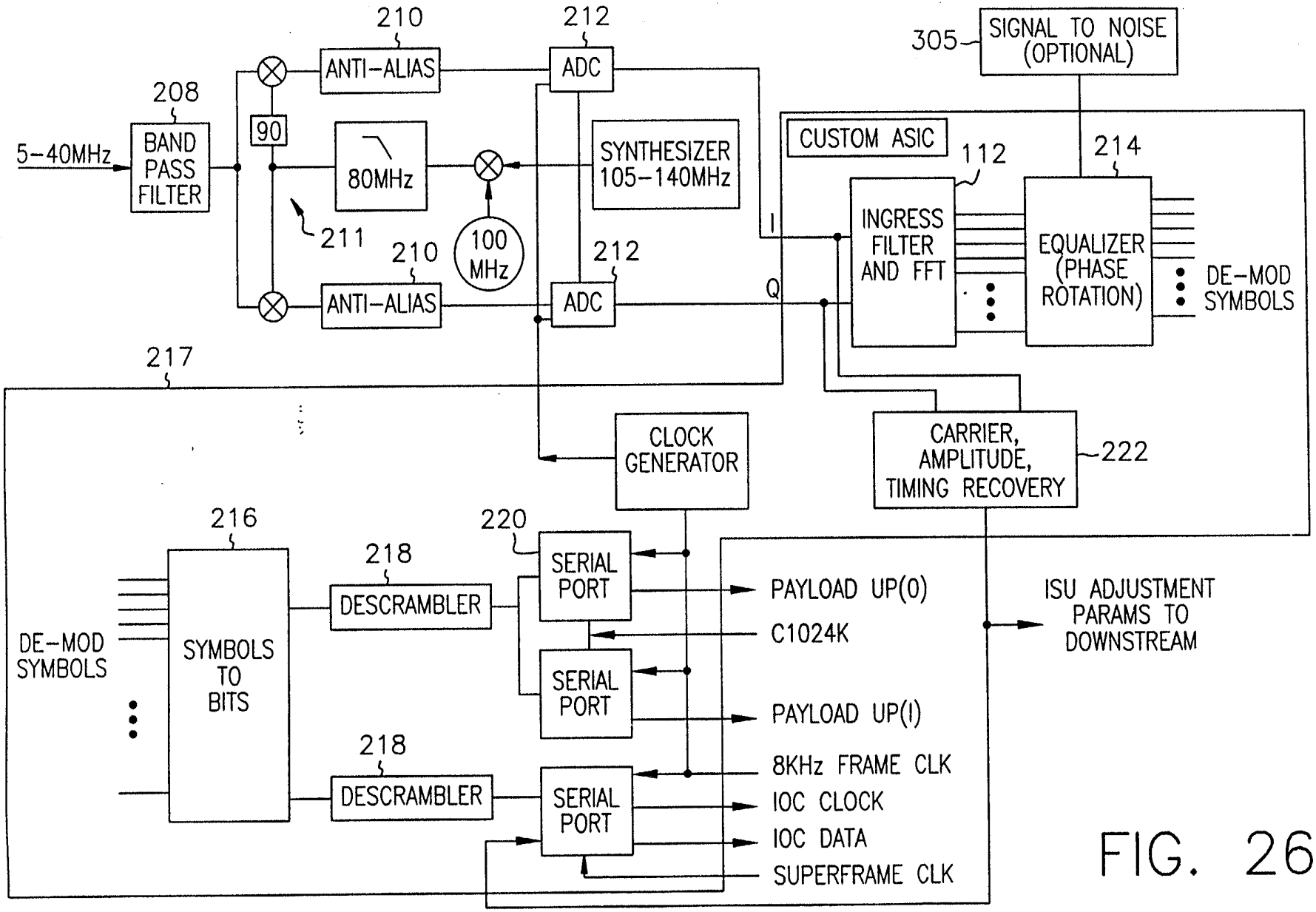

210
212
305
SIGNAL TO NOISE (OPTIONAL)
208
ANTI-ALIAS
ADC
CUSTOM ASIC
5-40MHz
BAND PASS FILTER
90
80MHz
SYNTHESIZER 105-140MHz
112
214
211
100 MHz
I
INGRESS FILTER AND FFT
EQUALIZER (PHASE ROTATION)
DE-MOD SYMBOLS
210
212
ANTI-ALIAS
ADC
Q
217
CLOCK GENERATOR
CARRIER, AMPLITUDE, TIMING RECOVERY
222
216
220
218
SERIAL PORT
DESCRAMBLER
PAYLOAD UP(0)
ISU ADJUSTMENT PARAMS TO DOWNSTREAM
DE-MOD SYMBOLS
SYMBOLS TO BITS
C1024K
SERIAL PORT
PAYLOAD UP(I)
218
8KHz FRAME CLK
DESCRAMBLER
SERIAL PORT
IOC CLOCK
IOC DATA
SUPERFRAME CLK

FIG. 26

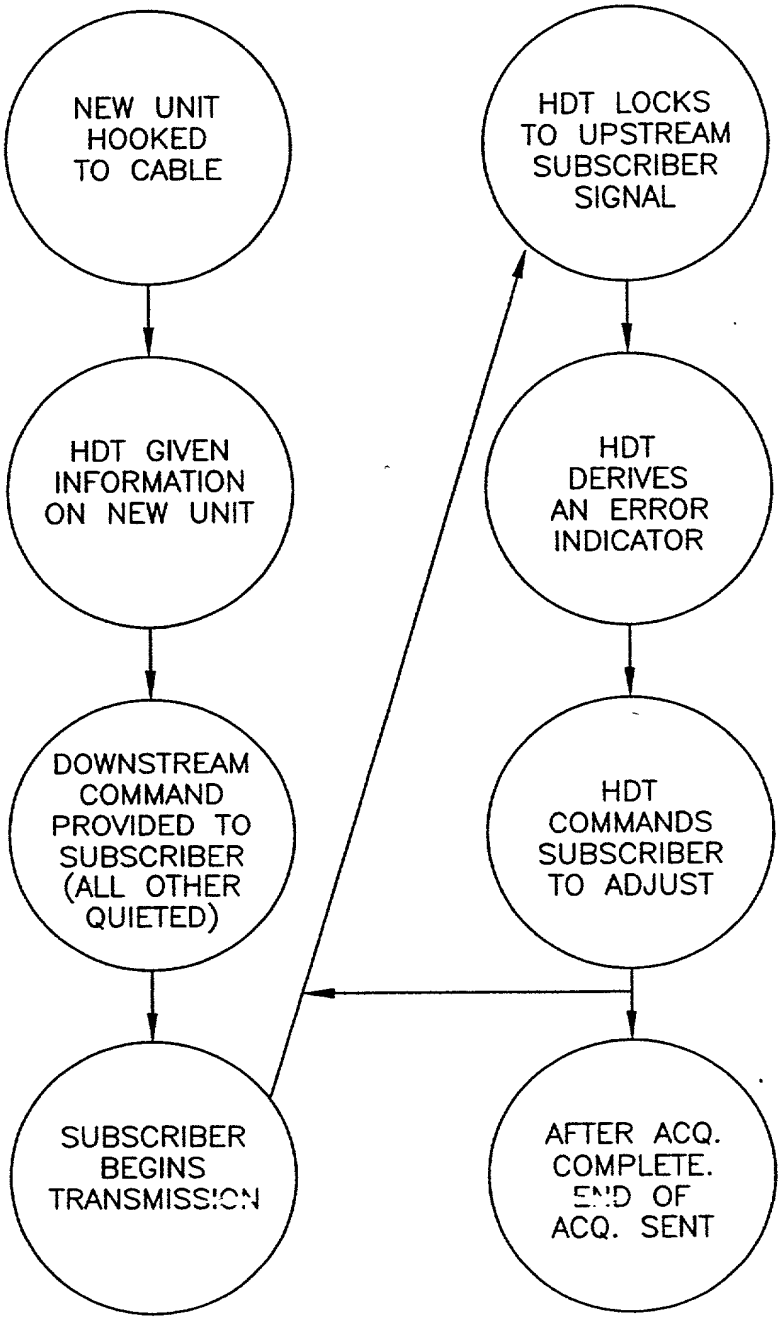


FIG. 27

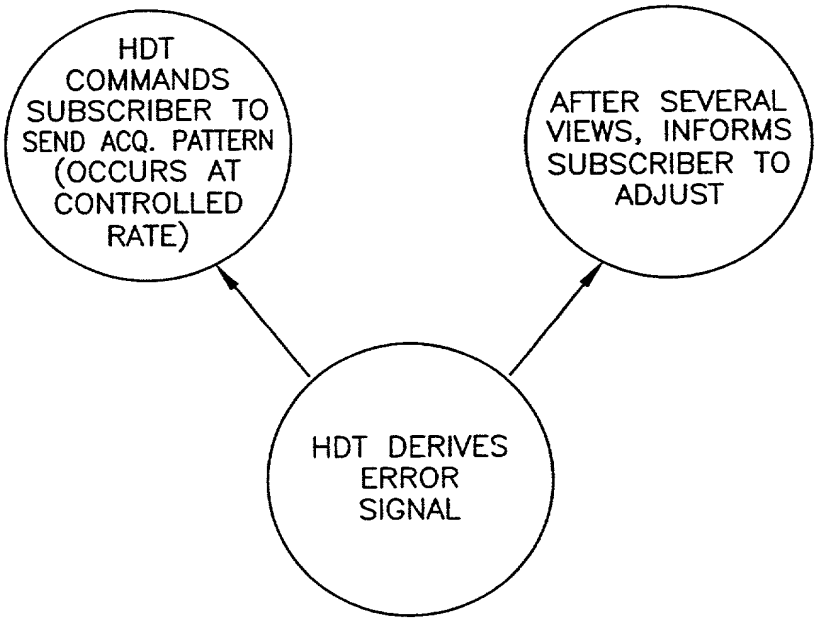


FIG. 28

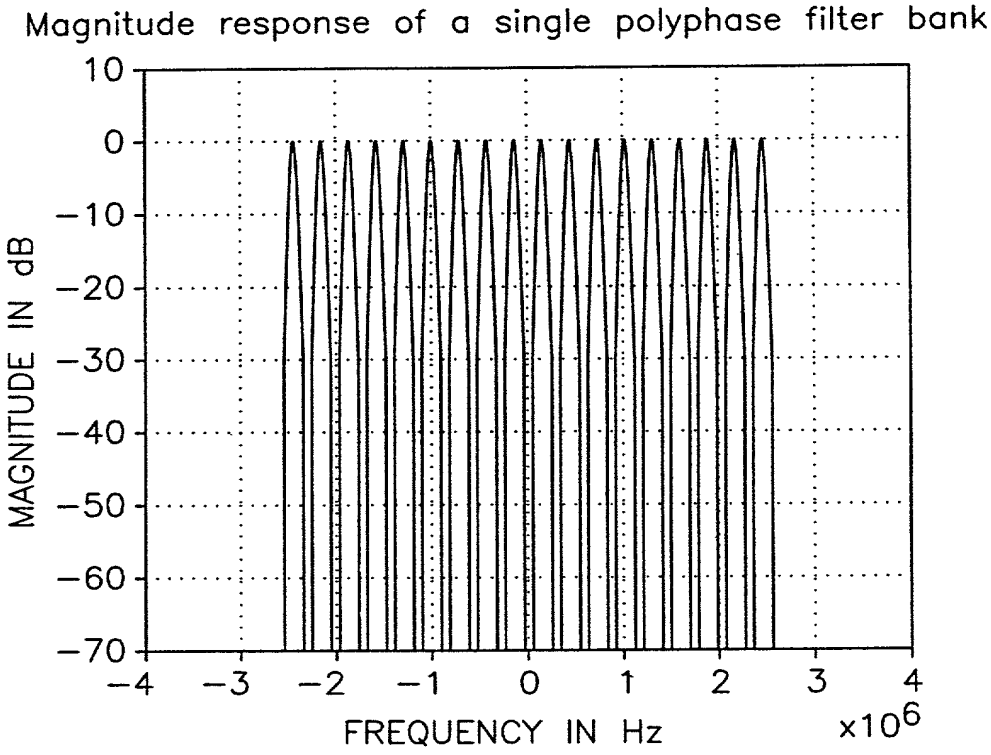

Magnitude response of a single polyphase filter bank
10
0
−10
−20
−30
−40
−50
−60
−70
MAGNITUDE IN dB
−4
−3
−2
−1
0
1
2
3
4
FREQUENCY IN Hz
x10^6

FIG. 29

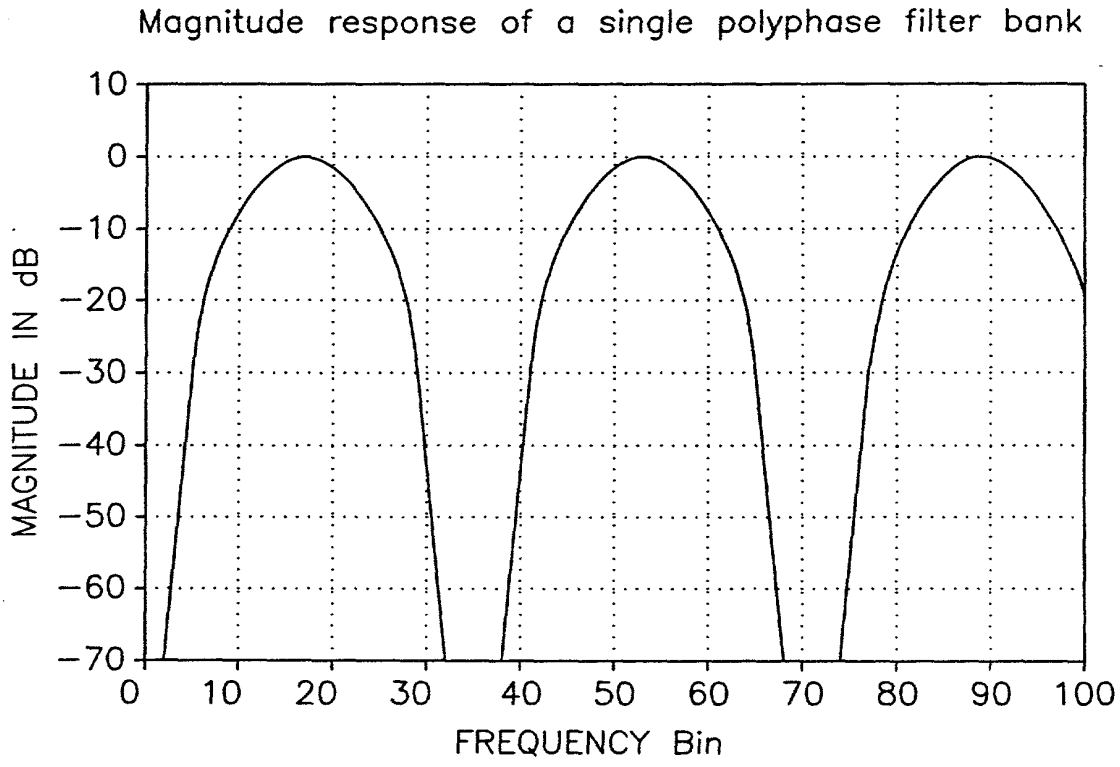

Magnitude response of a single polyphase filter bank
MAGNITUDE IN dB
10
0
−10
−20
−30
−40
−50
−60
−70
0
10
20
30
40
50
60
70
80
90
100
FREQUENCY Bin

FIG. 30

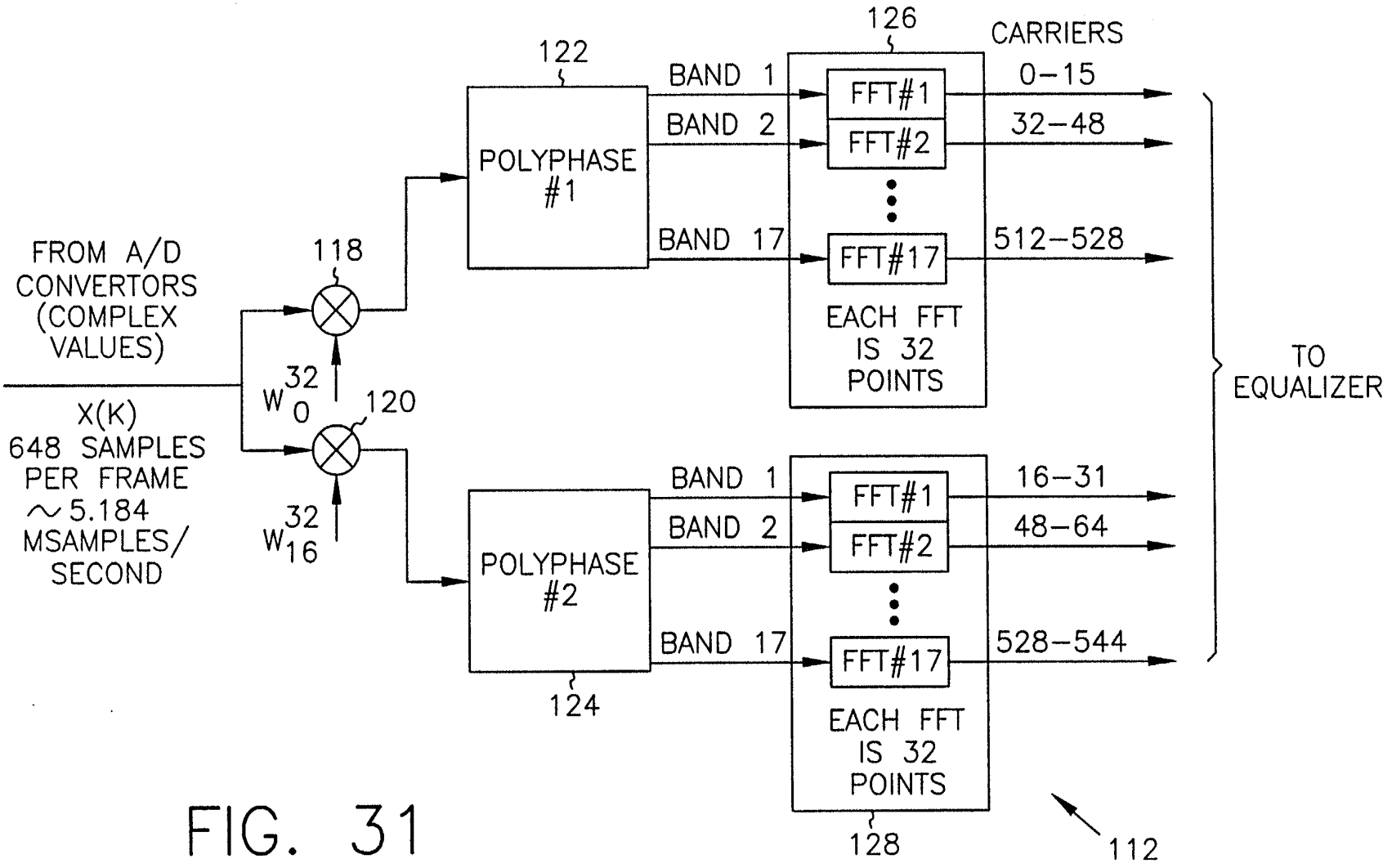

FROM A/D CONVERTORS (COMPLEX VALUES)
X(K)
648 SAMPLES PER FRAME
~5.184 MSAMPLES/ SECOND
118
120
W_0^{32}
W_{16}^{32}
122
POLYPHASE #1
124
POLYPHASE #2
126
BAND 1
BAND 2
BAND 17
FFT#1
FFT#2
FFT#17
EACH FFT IS 32 POINTS
128
CARRIERS
0–15
32–48
512–528
16–31
48–64
528–544
TO EQUALIZER
112

FIG. 31

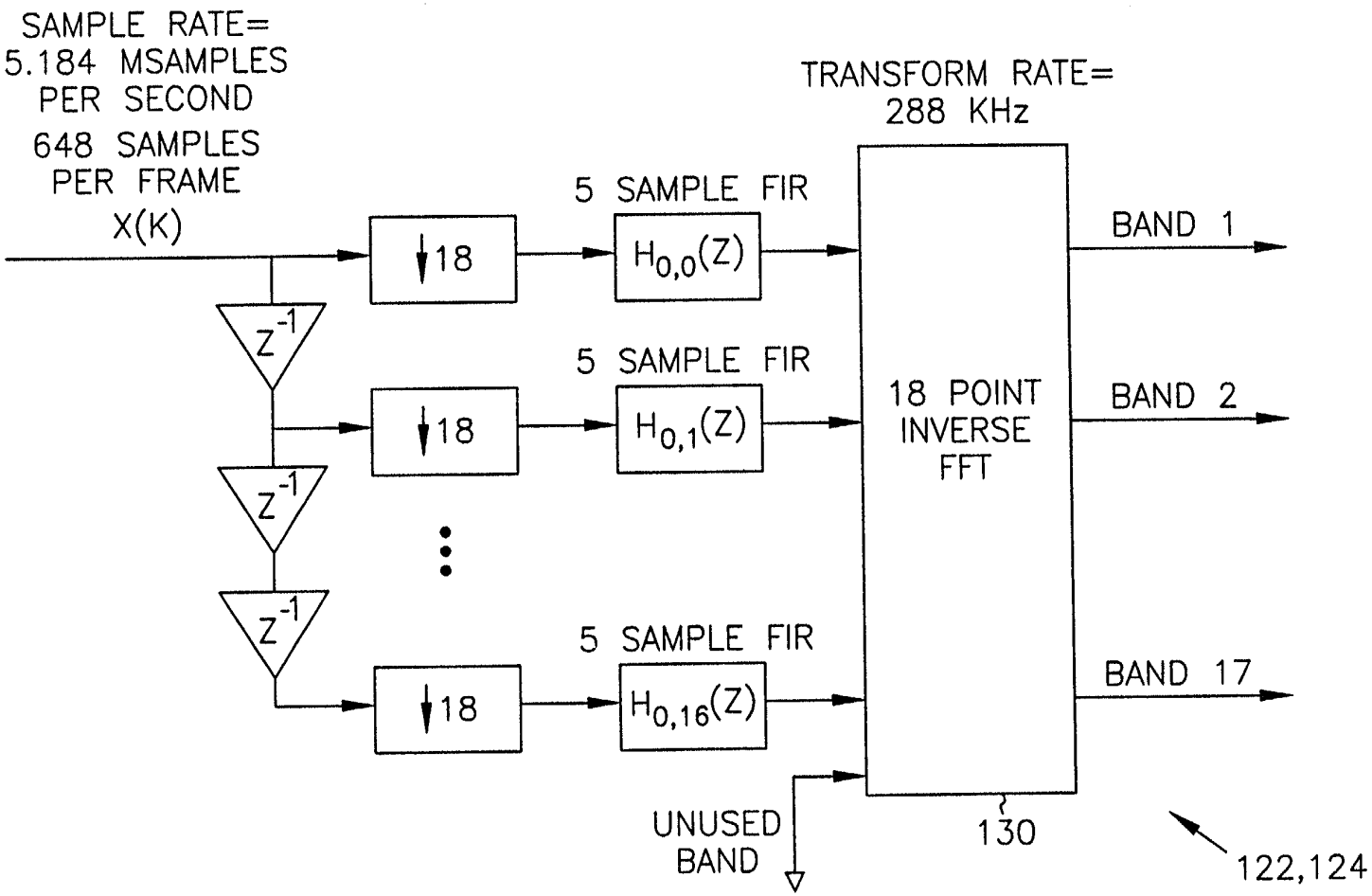


FIG. 32

FIG. 33

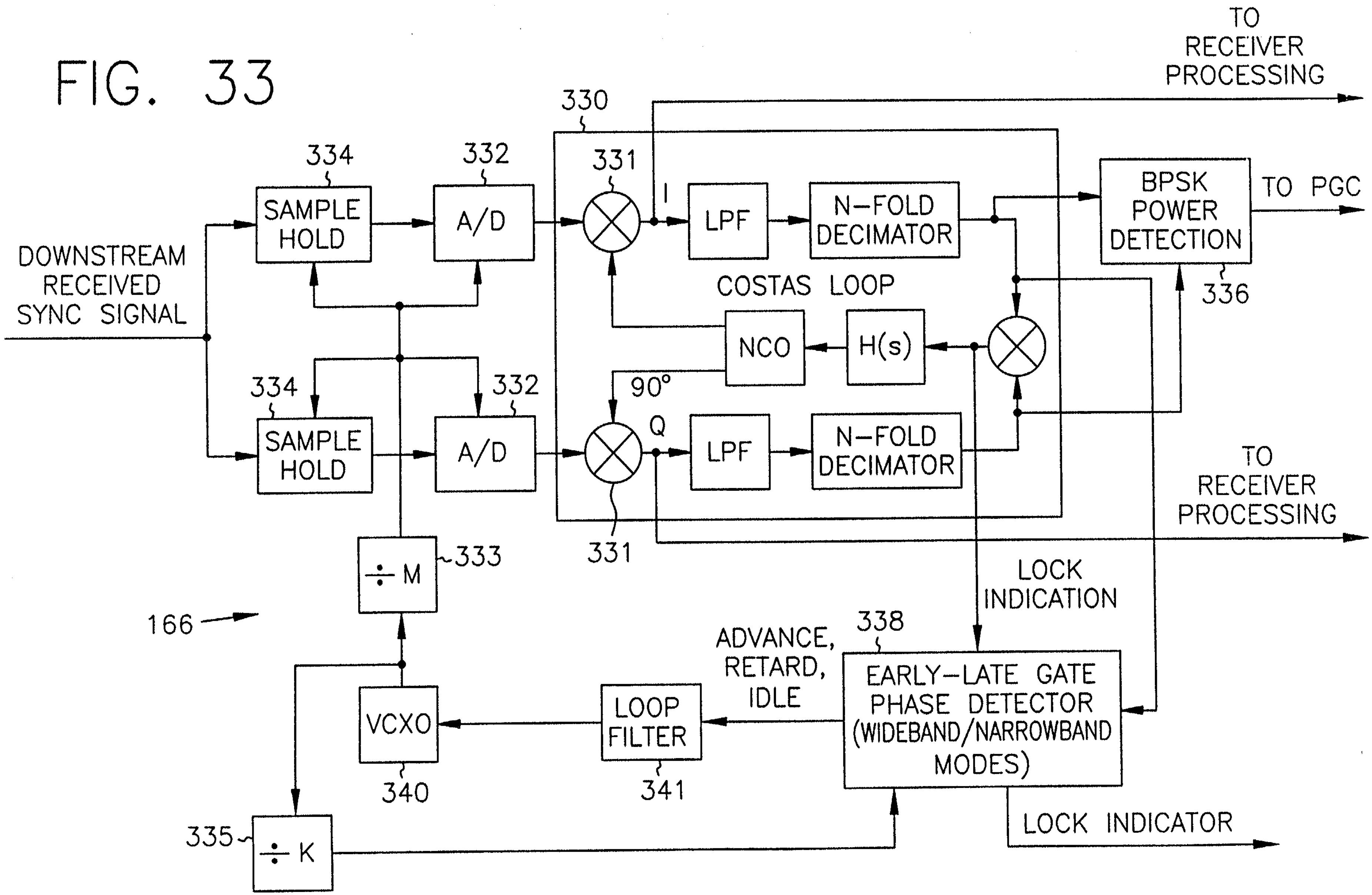
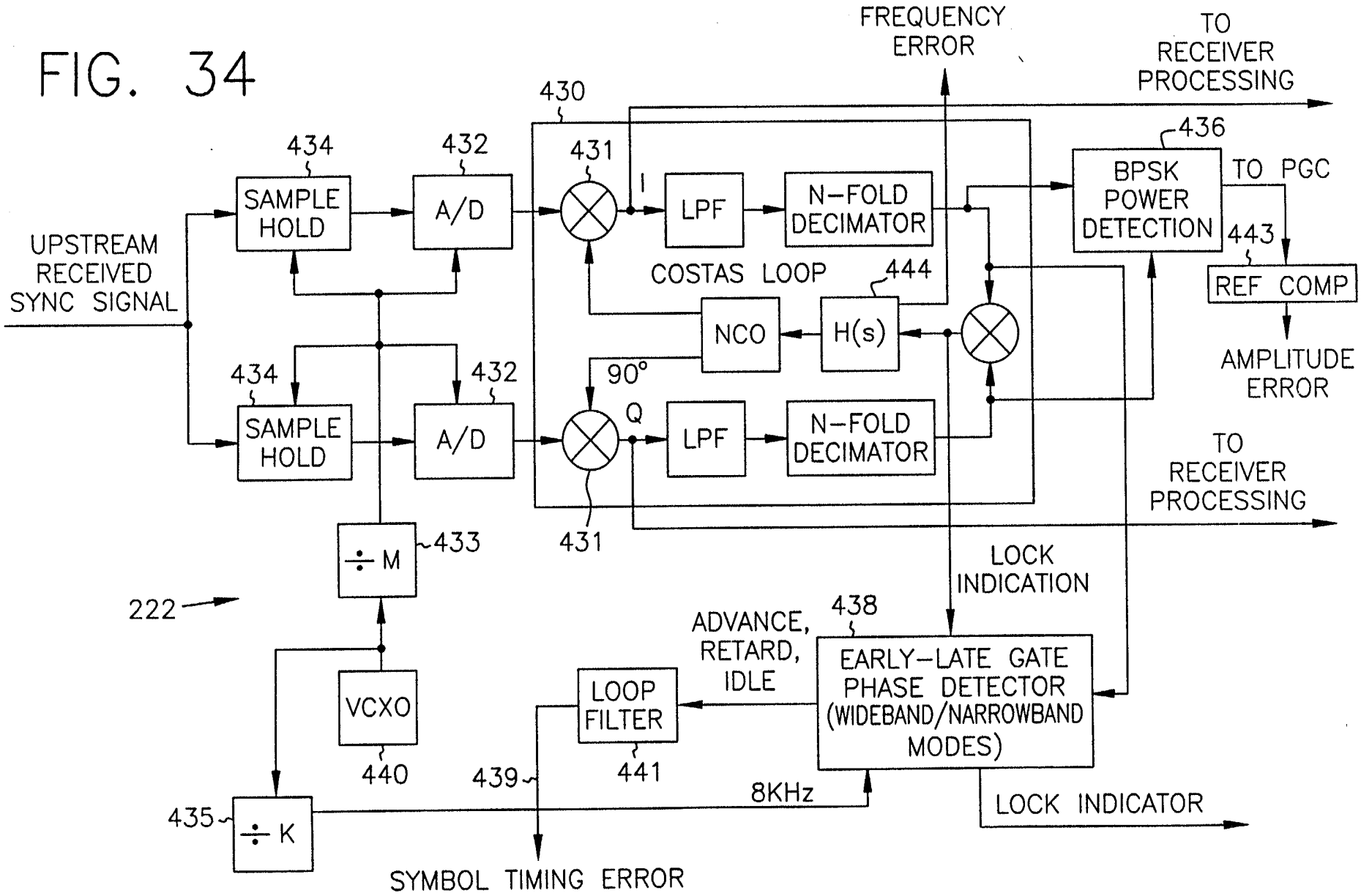

DOWNSTREAM RECEIVED SYNC SIGNAL
SAMPLE HOLD
334
A/D
332
330
331
I
Q
90°
LPF
N-FOLD DECIMATOR
COSTAS LOOP
NCO
H(s)
BPSK POWER DETECTION
336
TO PGC
TO RECEIVER PROCESSING
÷ M
333
166
VCXO
340
LOOP FILTER
341
ADVANCE, RETARD, IDLE
EARLY-LATE GATE PHASE DETECTOR (WIDEBAND/NARROWBAND MODES)
338
LOCK INDICATION
LOCK INDICATOR
÷ K
335

FIG. 34


FREQUENCY ERROR
TO RECEIVER PROCESSING
430
436
434
432
431
I
SAMPLE HOLD
A/D
LPF
N-FOLD DECIMATOR
BPSK POWER DETECTION
TO PGC
443
UPSTREAM RECEIVED SYNC SIGNAL
COSTAS LOOP
444
REF COMP
NCO
H(s)
AMPLITUDE ERROR
90°
Q
TO RECEIVER PROCESSING
÷ M
433
LOCK INDICATION
222
ADVANCE, RETARD, IDLE
438
EARLY-LATE GATE PHASE DETECTOR (WIDEBAND/NARROWBAND MODES)
VCXO
LOOP FILTER
440
439
441
8KHz
LOCK INDICATOR
435
÷ K
SYMBOL TIMING ERROR

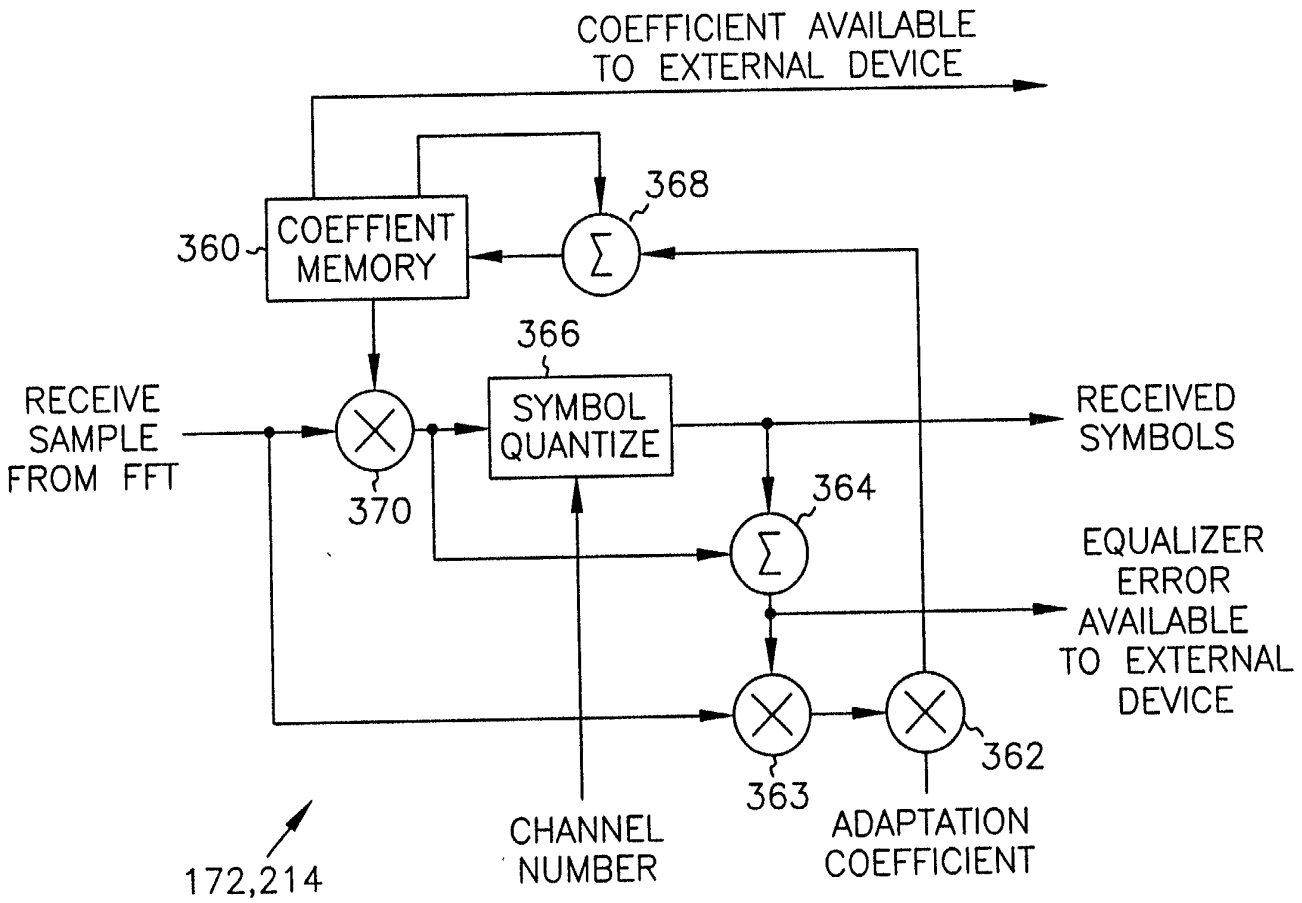
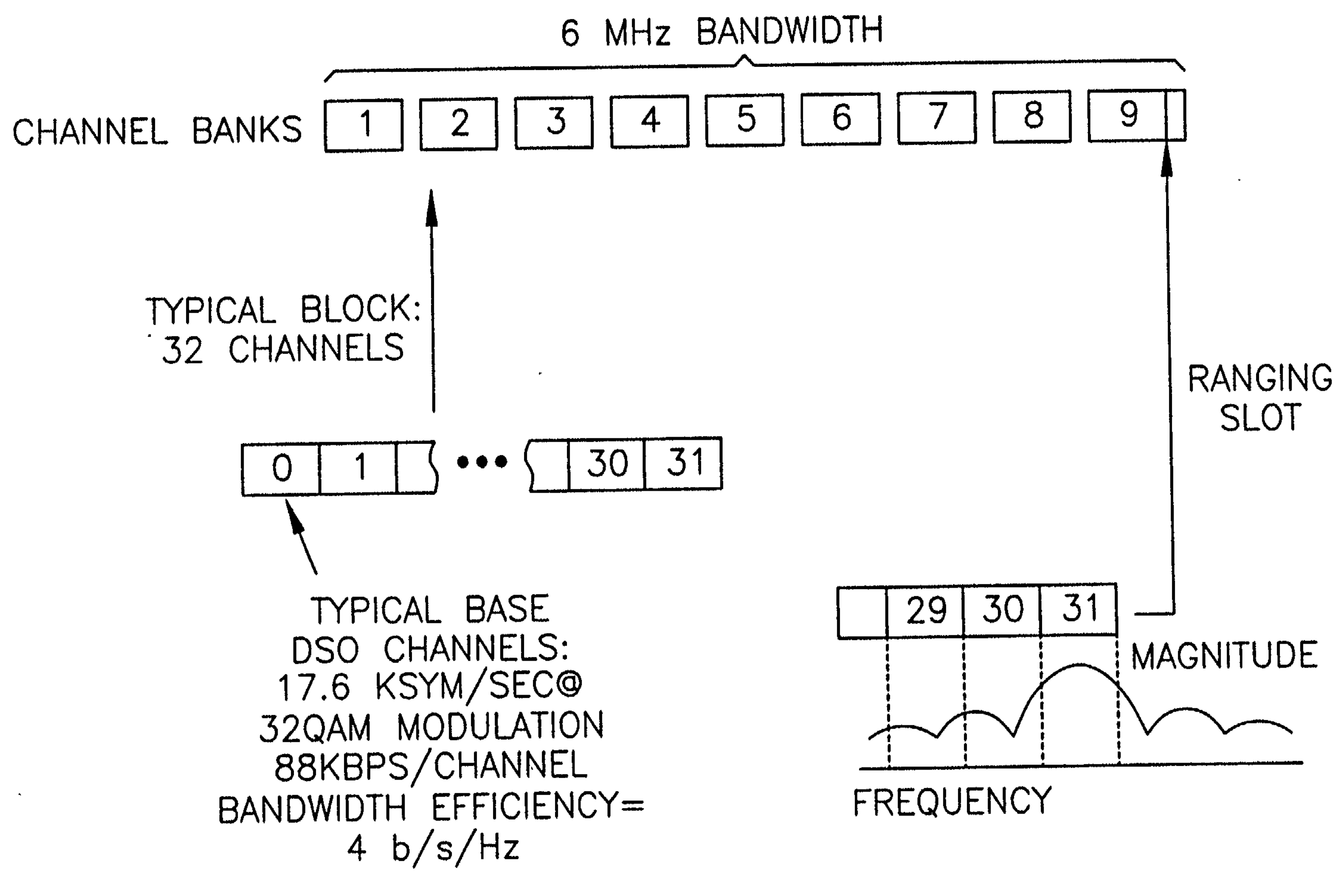

COEFFICIENT AVAILABLE
TO EXTERNAL DEVICE
368
360
COEFFIENT
MEMORY
366
SYMBOL
QUANTIZE
RECEIVE
SAMPLE
FROM FFT
370
RECEIVED
SYMBOLS
364
EQUALIZER
ERROR
AVAILABLE
TO EXTERNAL
DEVICE
362
363
172,214
CHANNEL
NUMBER
ADAPTATION
COEFFICIENT

FIG. 35



6 MHz BANDWIDTH
CHANNEL BANKS
1
2
3
4
5
6
7
8
9
TYPICAL BLOCK:
32 CHANNELS
0
1
30
31
RANGING
SLOT
TYPICAL BASE
DSO CHANNELS:
17.6 KSYM/SEC@
32QAM MODULATION
88KBPS/CHANNEL
BANDWIDTH EFFICIENCY=
4 b/s/Hz
29
30
31
MAGNITUDE
FREQUENCY

FIG. 36

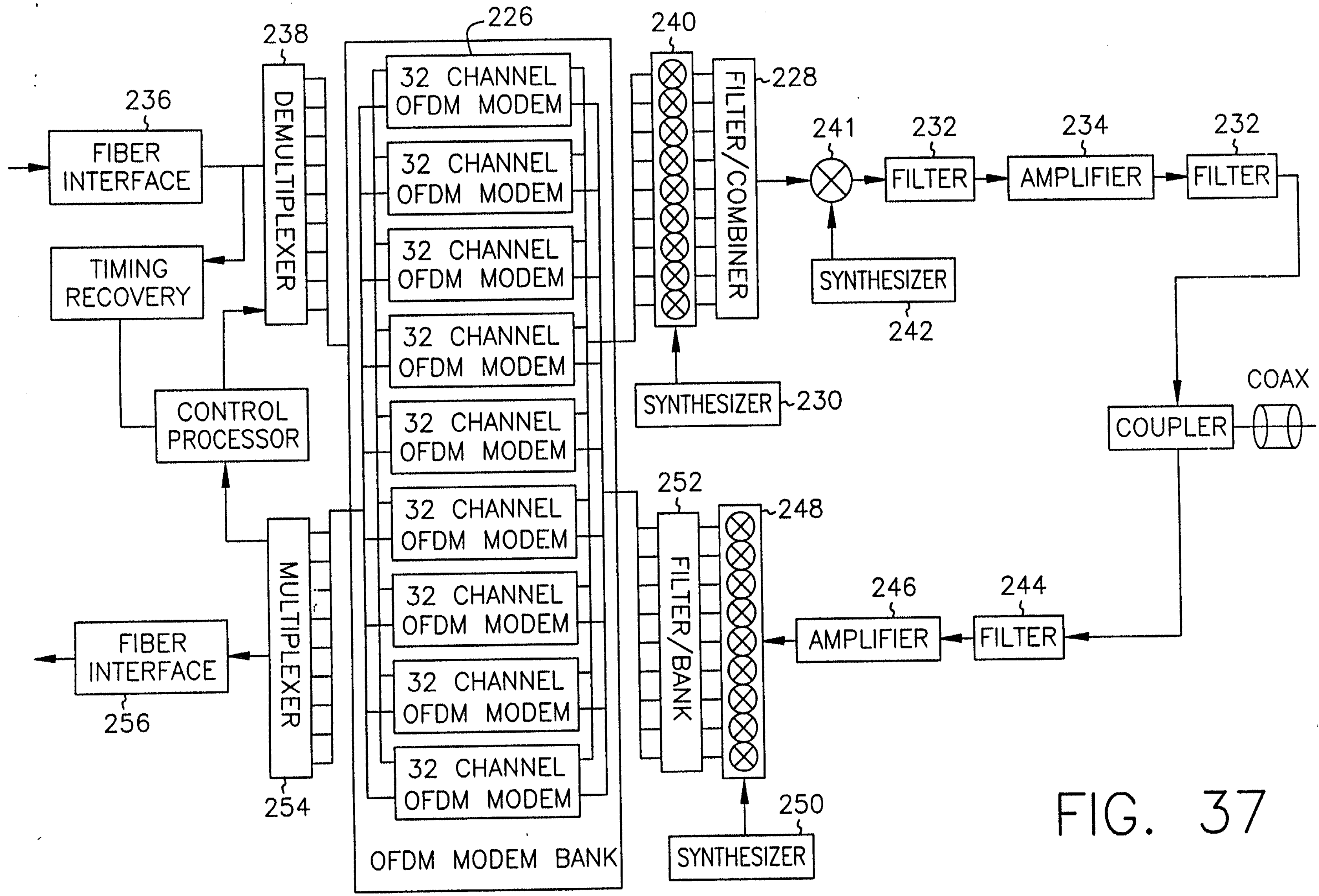
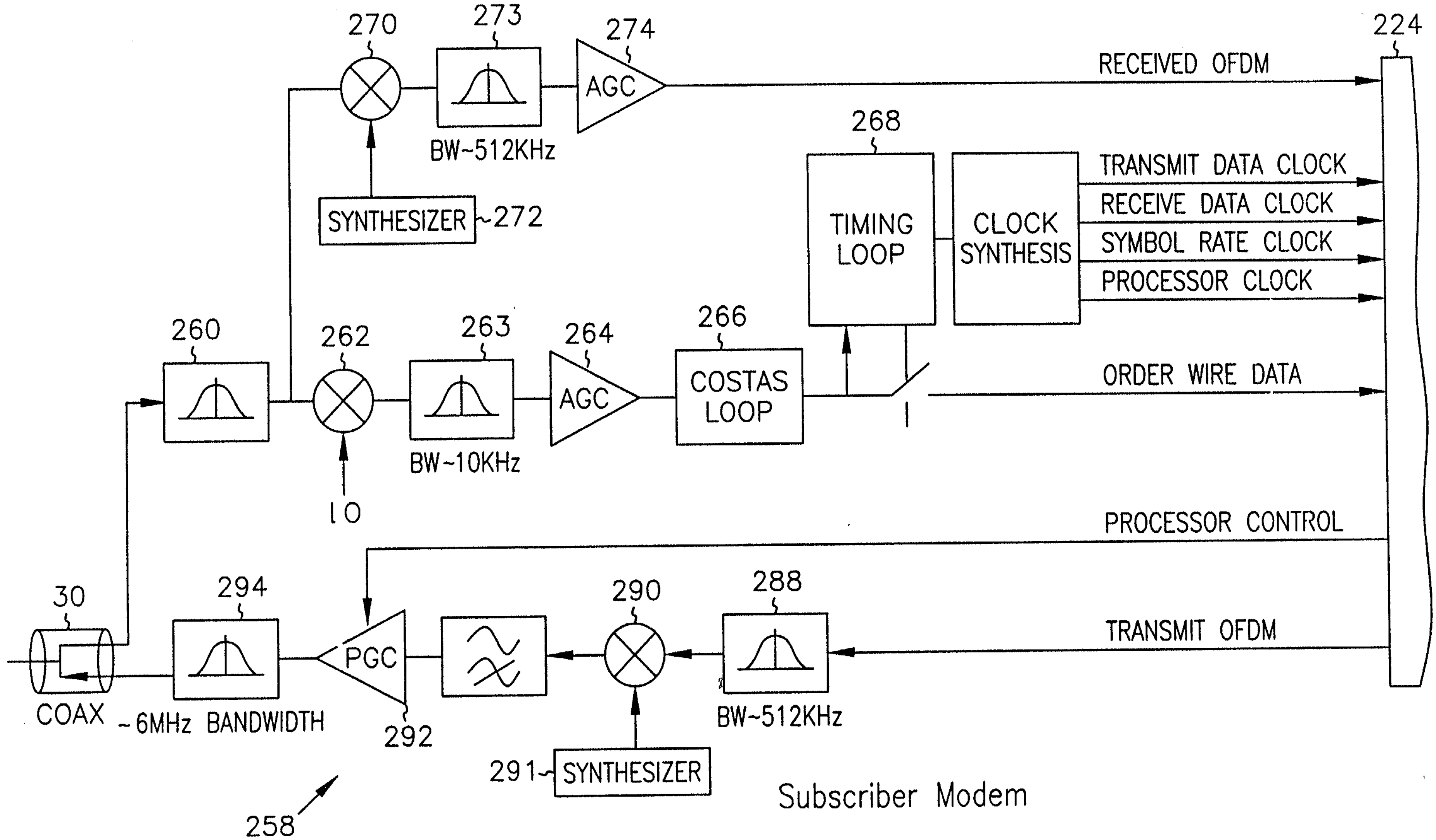

FIBER INTERFACE
236
TIMING RECOVERY
CONTROL PROCESSOR
DEMULTIPLEXER
238
MULTIPLEXER
254
FIBER INTERFACE
256
226
32 CHANNEL OFDM MODEM
OFDM MODEM BANK
240
FILTER/COMBINER
228
SYNTHESIZER
230
241
SYNTHESIZER
242
FILTER
232
AMPLIFIER
234
COAX
COUPLER
252
FILTER/BANK
248
SYNTHESIZER
250
AMPLIFIER
246
FILTER
244

FIG. 37



Subscriber Modem

FIG. 38

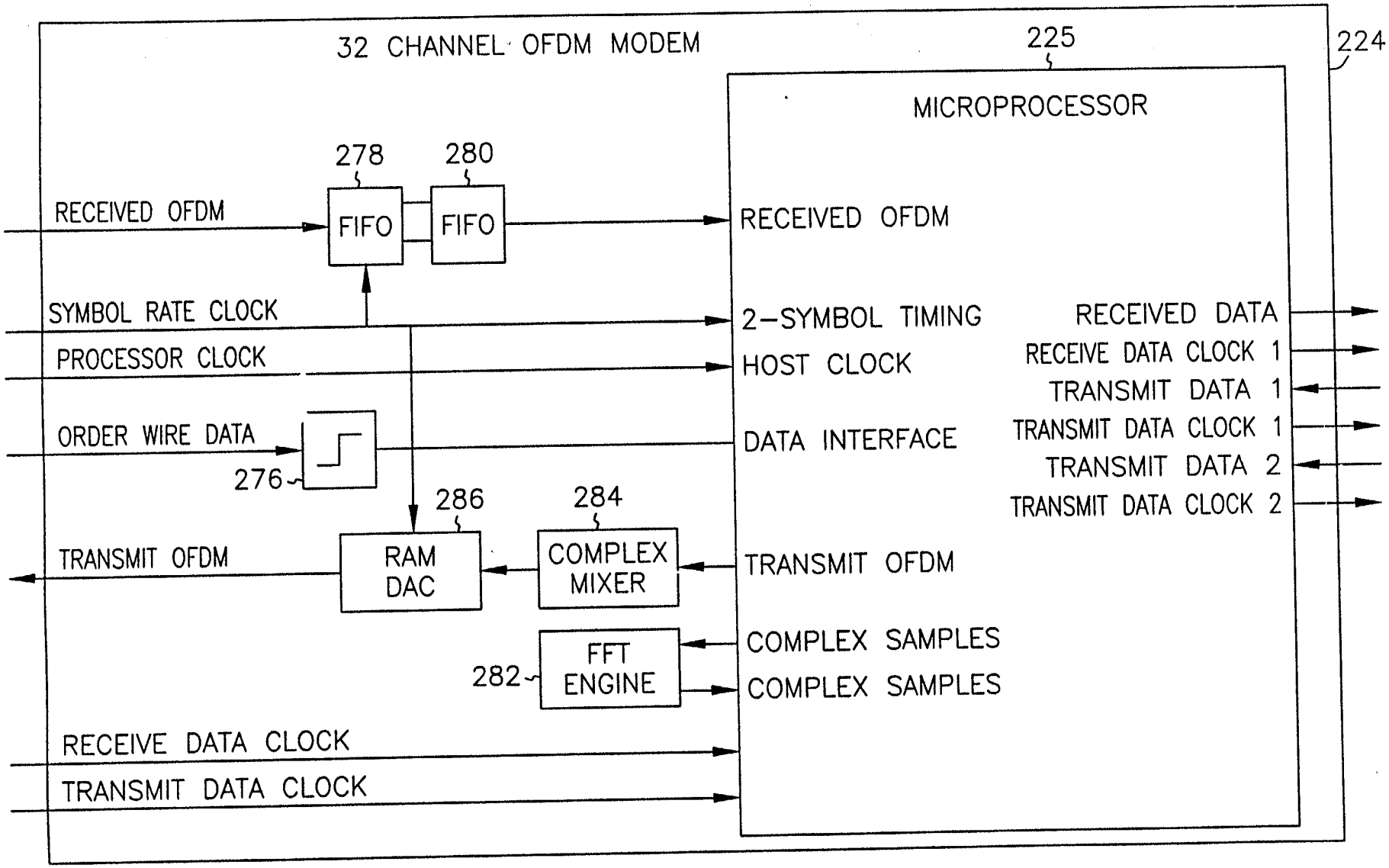

32 CHANNEL OFDM MODEM
225
224
MICROPROCESSOR
278
280
RECEIVED OFDM
FIFO
FIFO
RECEIVED OFDM
SYMBOL RATE CLOCK
2-SYMBOL TIMING
RECEIVED DATA
PROCESSOR CLOCK
HOST CLOCK
RECEIVE DATA CLOCK 1
TRANSMIT DATA 1
ORDER WIRE DATA
DATA INTERFACE
TRANSMIT DATA CLOCK 1
TRANSMIT DATA 2
276
286
284
TRANSMIT OFDM
RAM DAC
COMPLEX MIXER
TRANSMIT OFDM
TRANSMIT DATA CLOCK 2
COMPLEX SAMPLES
FFT ENGINE
282
COMPLEX SAMPLES
RECEIVE DATA CLOCK
TRANSMIT DATA CLOCK

FIG. 39

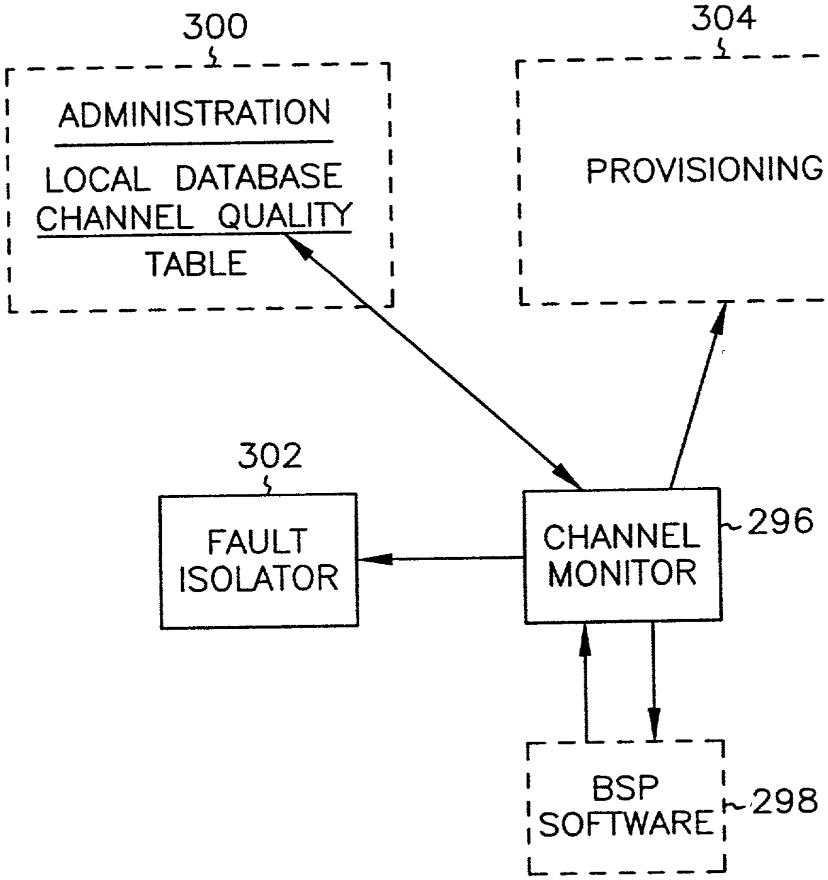


FIG. 40

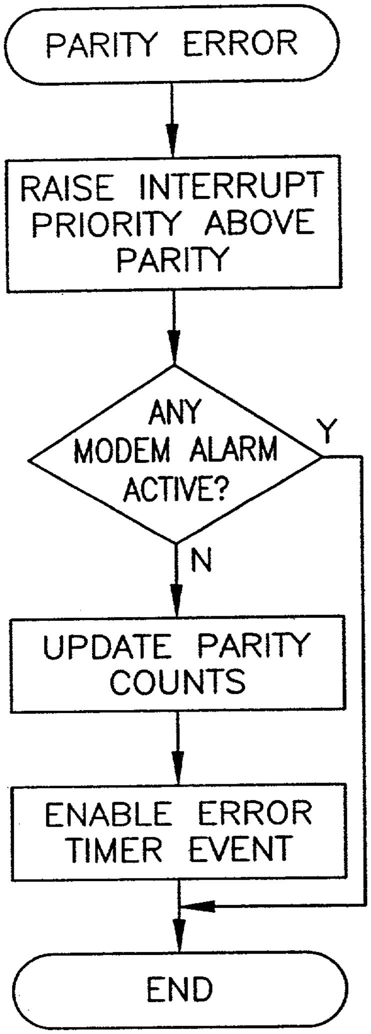


FIG. 41

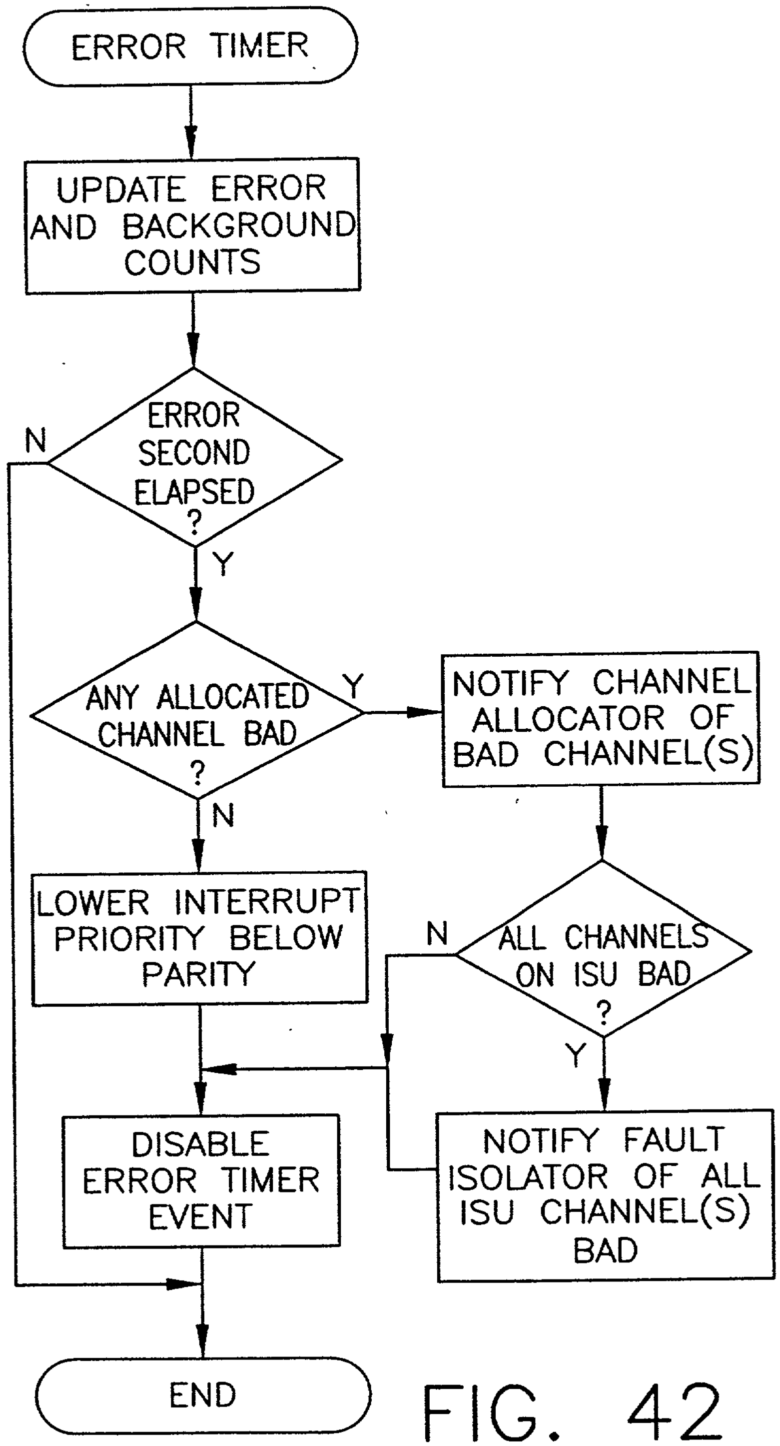


FIG. 42

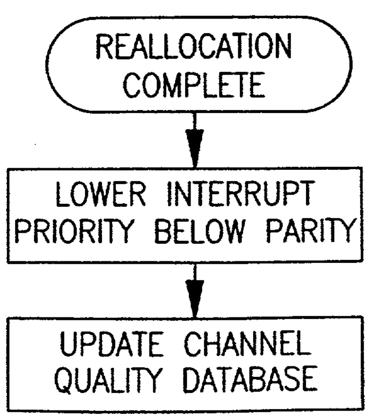
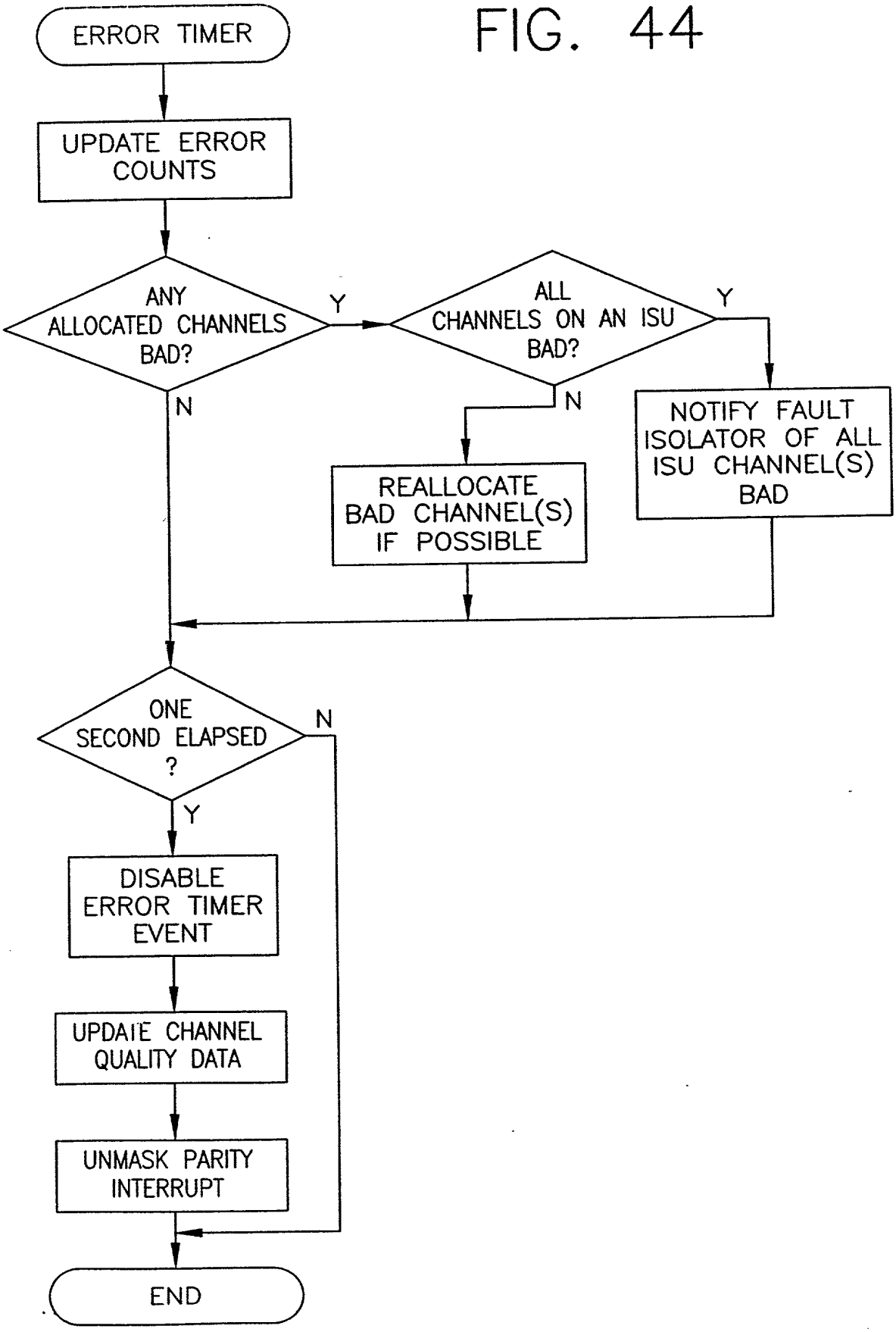


FIG. 43

FIG. 44


ERROR TIMER
UPDATE ERROR COUNTS
ANY ALLOCATED CHANNELS BAD?
Y
ALL CHANNELS ON AN ISU BAD?
Y
N
N
NOTIFY FAULT ISOLATOR OF ALL ISU CHANNEL(S) BAD
REALLOCATE BAD CHANNEL(S) IF POSSIBLE
ONE SECOND ELAPSED ?
N
Y
DISABLE ERROR TIMER EVENT
UPDATE CHANNEL QUALITY DATA
UNMASK PARITY INTERRUPT
END

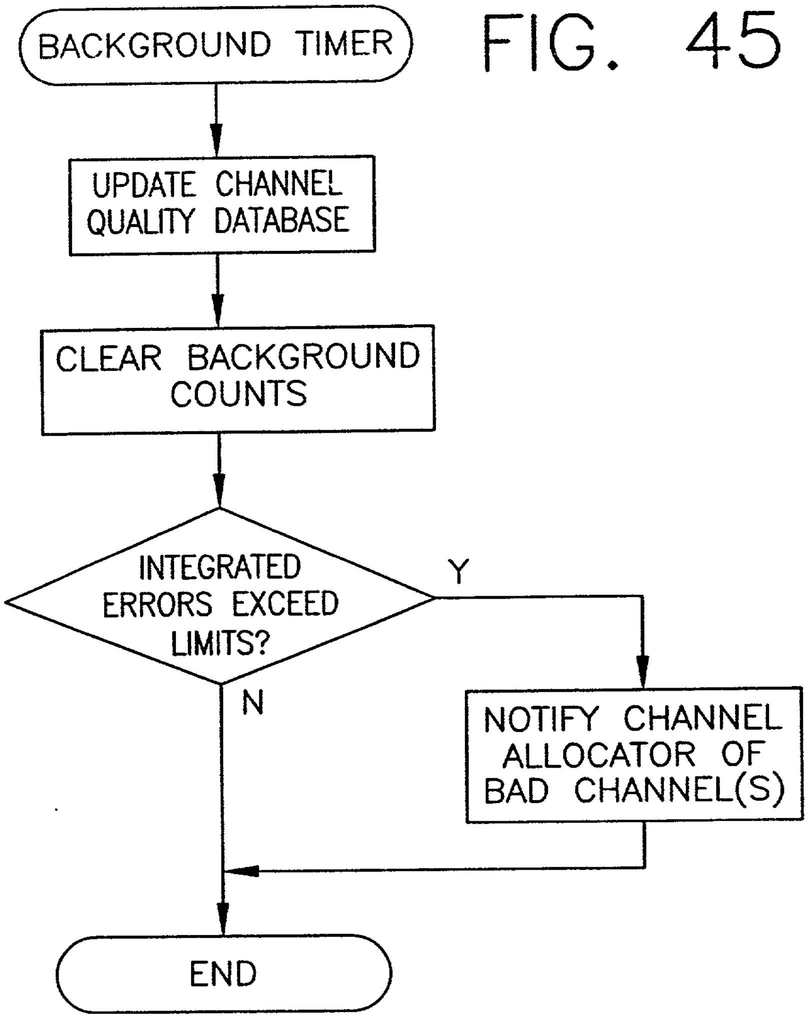


FIG. 45

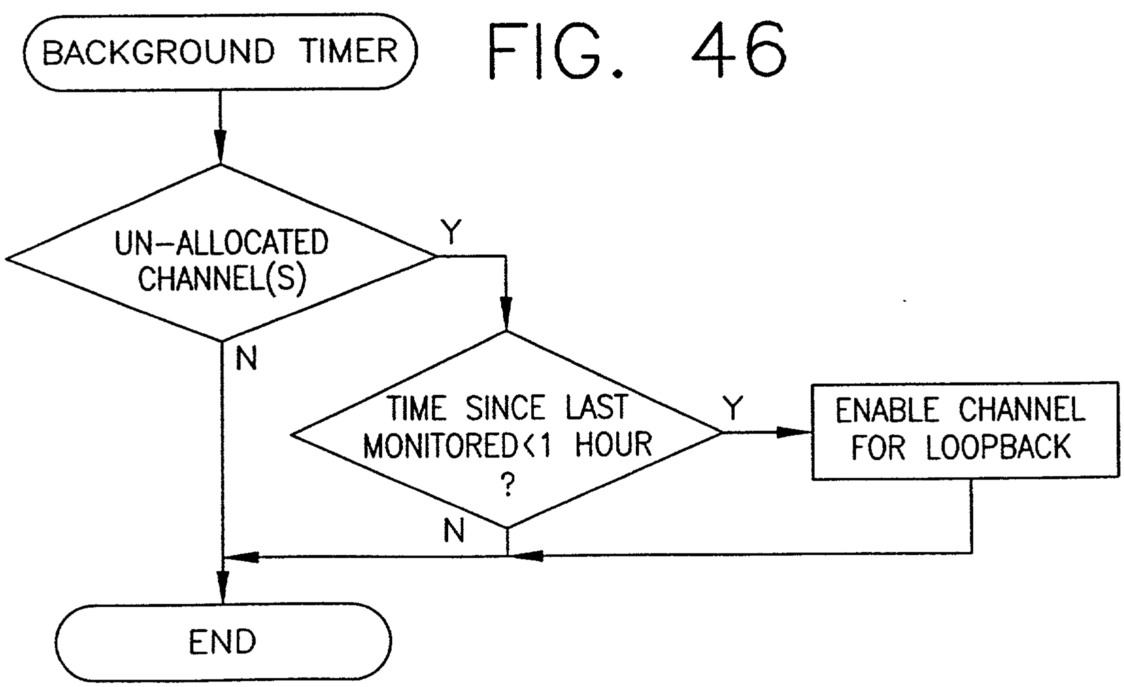


FIG. 46

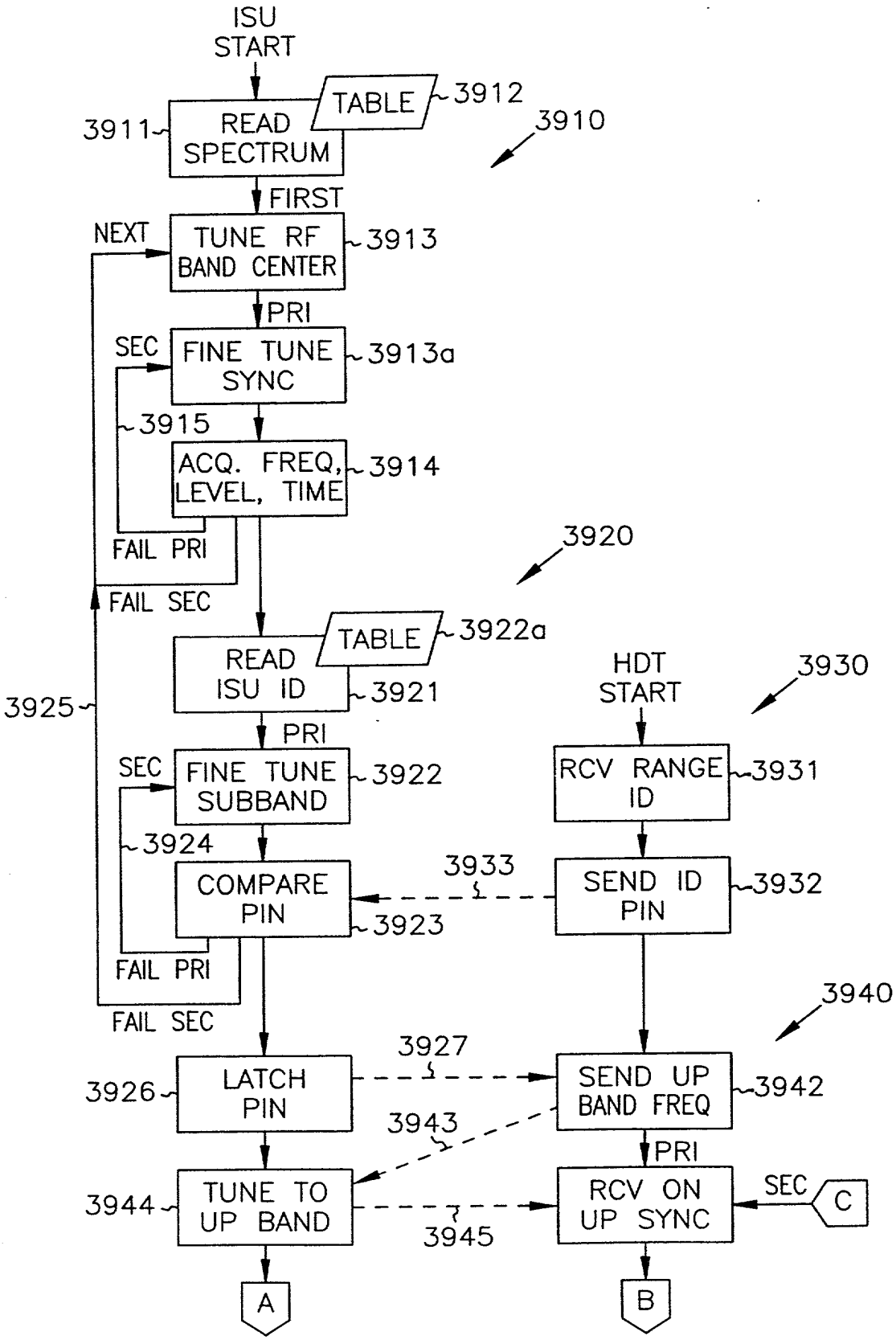

ISU START
TABLE
3912
3911
READ SPECTRUM
3910
FIRST
NEXT
TUNE RF BAND CENTER
3913
PRI
SEC
FINE TUNE SYNC
3913a
3915
ACQ. FREQ, LEVEL, TIME
3914
FAIL PRI
FAIL SEC
3920
TABLE
3922a
READ ISU ID
3921
3925
PRI
SEC
FINE TUNE SUBBAND
3922
3924
COMPARE PIN
3923
FAIL PRI
FAIL SEC
HDT START
3930
RCV RANGE ID
3931
3933
SEND ID PIN
3932
3940
3927
3926
LATCH PIN
SEND UP BAND FREQ
3942
3943
PRI
3944
TUNE TO UP BAND
RCV ON UP SYNC
SEC
C
3945
A
B

FIG. 47

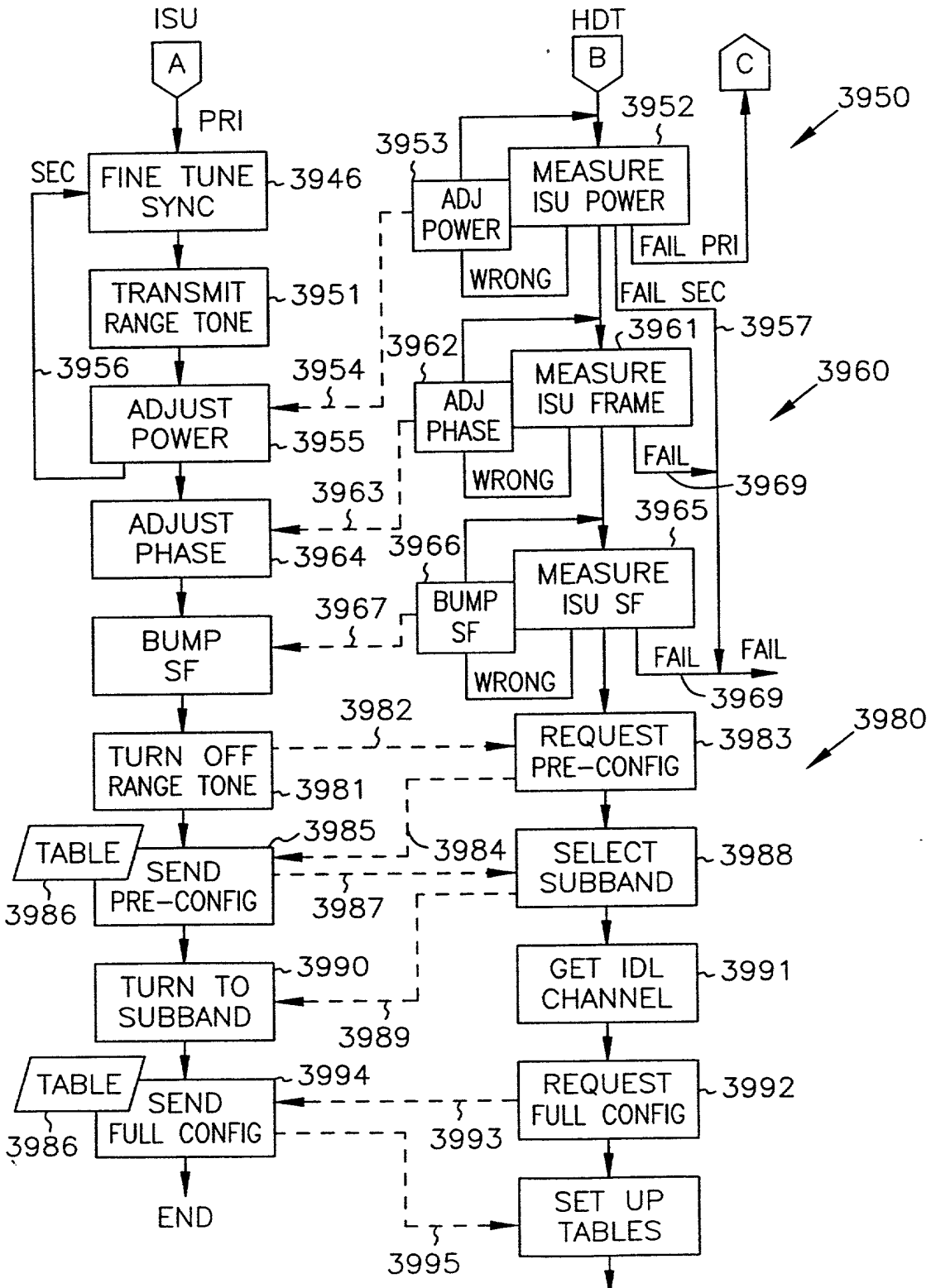

ISU
HDT
A
B
C
PRI
SEC
FINE TUNE SYNC
3946
TRANSMIT RANGE TONE
3951
ADJUST POWER
3955
ADJUST PHASE
3964
BUMP SF
TURN OFF RANGE TONE
3981
TABLE
SEND PRE-CONFIG
3986
TURN TO SUBBAND
3990
TABLE
SEND FULL CONFIG
3994
END
3956
3954
3963
3966
3967
3982
3985
3987
3989
3993
3995
3950
3952
3953
ADJ POWER
MEASURE ISU POWER
WRONG
FAIL PRI
FAIL SEC
3957
3961
3962
ADJ PHASE
MEASURE ISU FRAME
3960
WRONG
FAIL
3969
3965
BUMP SF
MEASURE ISU SF
WRONG
FAIL
FAIL
3969
3980
REQUEST PRE-CONFIG
3983
3984
SELECT SUBBAND
3988
GET IDL CHANNEL
3991
REQUEST FULL CONFIG
3992
SET UP TABLES
END

FIG. 48

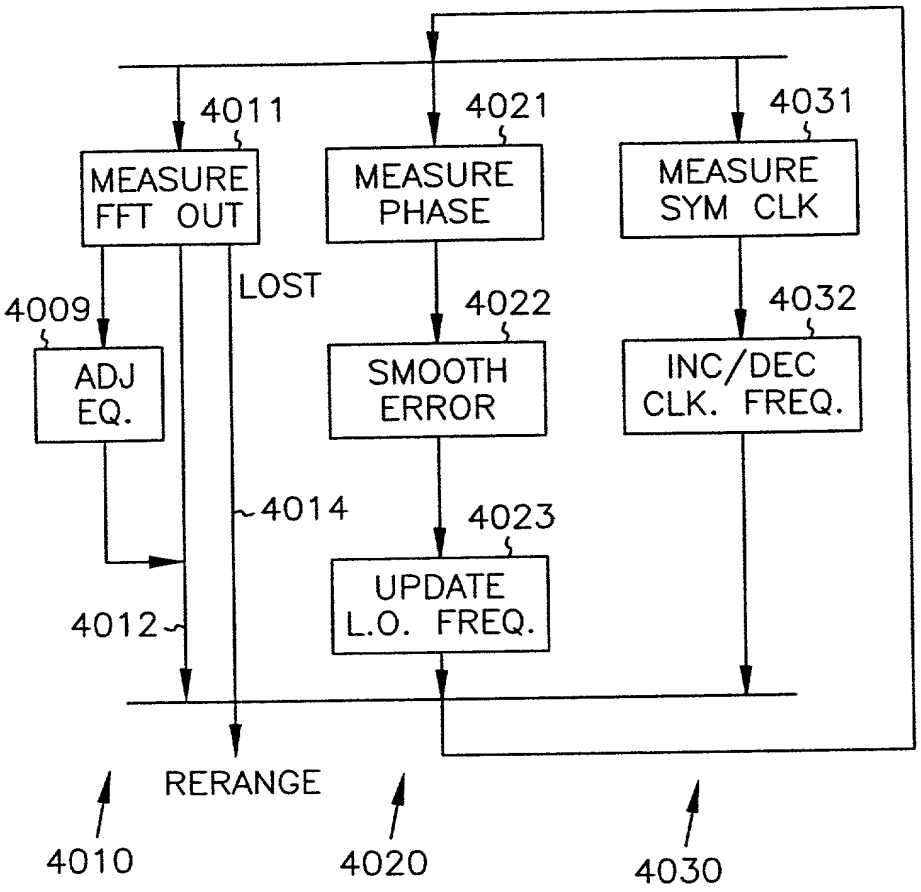

4011
4021
4031
MEASURE FFT OUT
MEASURE PHASE
MEASURE SYM CLK
LOST
4009
4022
4032
ADJ EQ.
SMOOTH ERROR
INC/DEC CLK. FREQ.
4014
4023
UPDATE L.O. FREQ.
4012
RERANGE
4010
4020
4030

FIG. 49

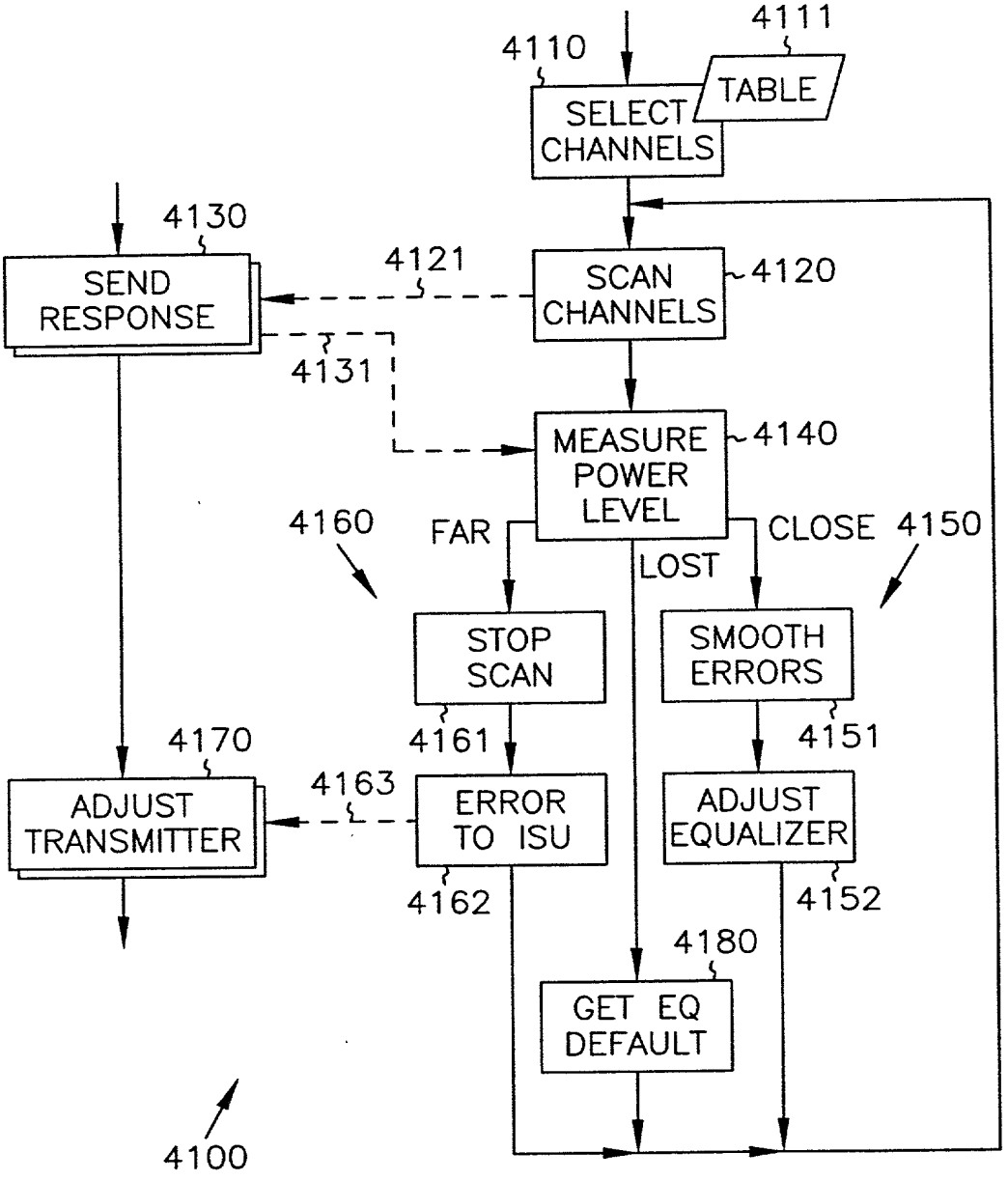

4111
4110
TABLE
SELECT CHANNELS
4130
SEND RESPONSE
4121
SCAN CHANNELS
4120
4131
MEASURE POWER LEVEL
4140
4160
FAR
CLOSE
4150
LOST
STOP SCAN
SMOOTH ERRORS
4170
4161
4151
ADJUST TRANSMITTER
4163
ERROR TO ISU
ADJUST EQUALIZER
4162
4152
4180
GET EQ DEFAULT
4100

FIG. 50

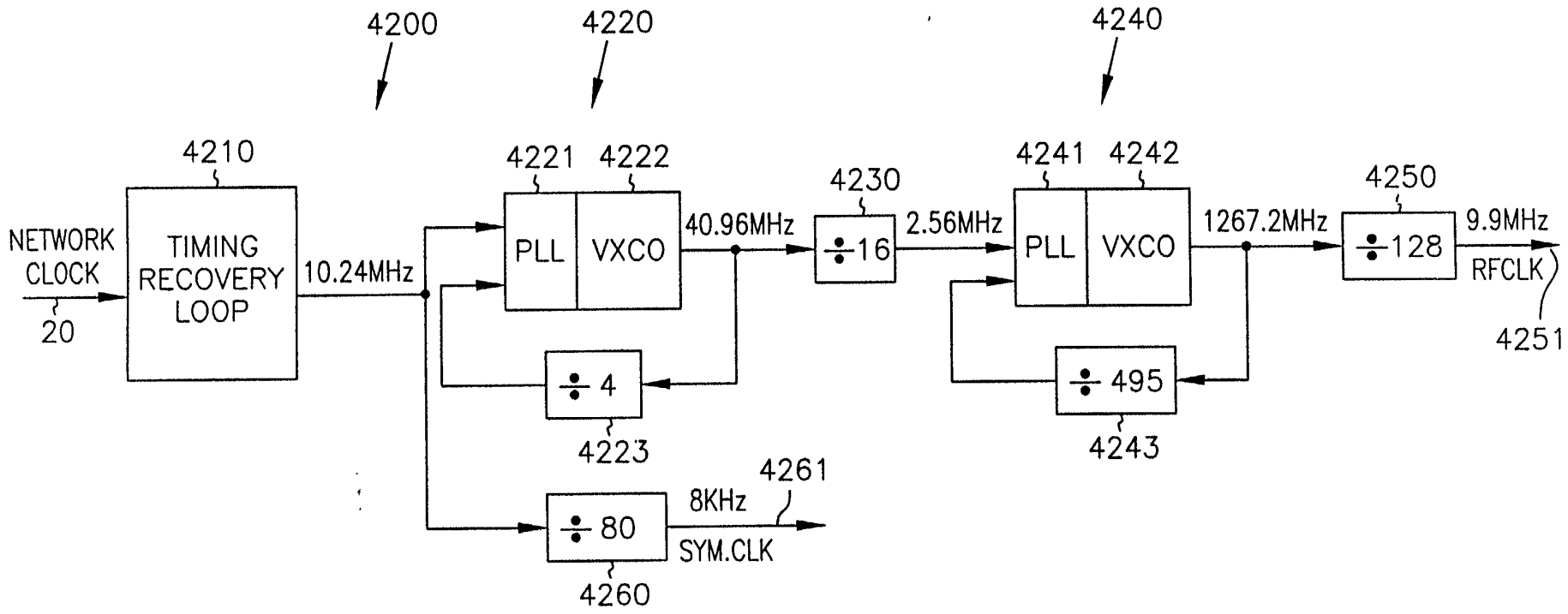

4200
4220
4240
4210
4221
4222
4230
4241
4242
4250
NETWORK CLOCK
20
TIMING RECOVERY LOOP
10.24MHz
PLL
VXCO
40.96MHz
÷16
2.56MHz
PLL
VXCO
1267.2MHz
÷128
9.9MHz
RFCLK
4251
÷ 4
4223
÷ 495
4243
4261
8KHz
÷ 80
SYM.CLK
4260

FIG. 51

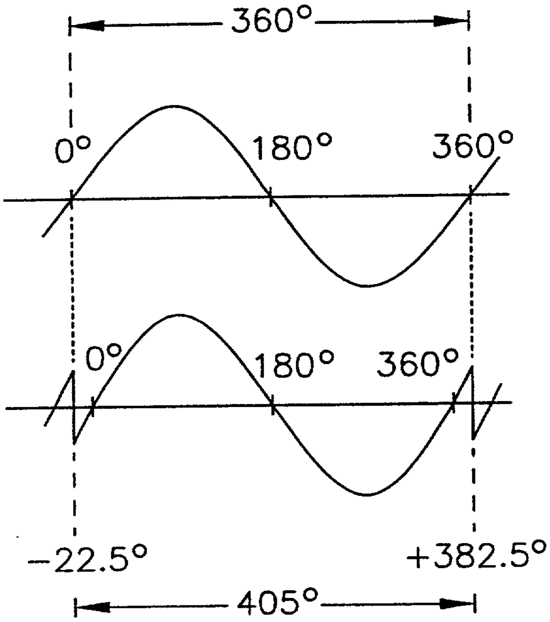

360°
0°
180°
360°
0°
180°
360°
−22.5°
+382.5°
405°

FIG. 52

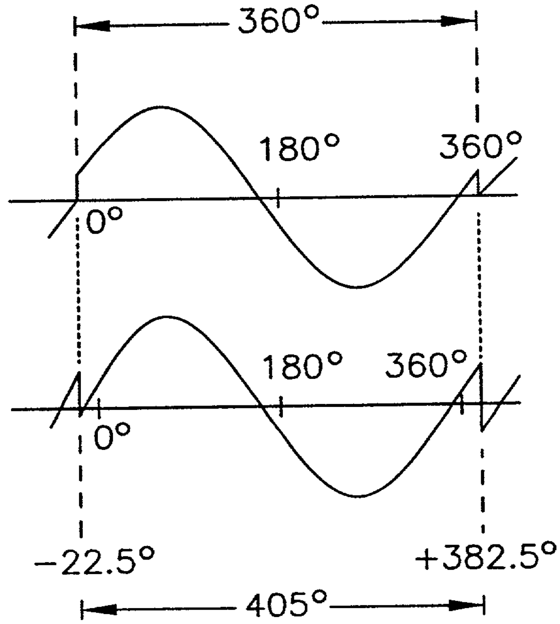

360°
180°
360°
0°
180°
360°
0°
−22.5°
+382.5°
405°

FIG. 53

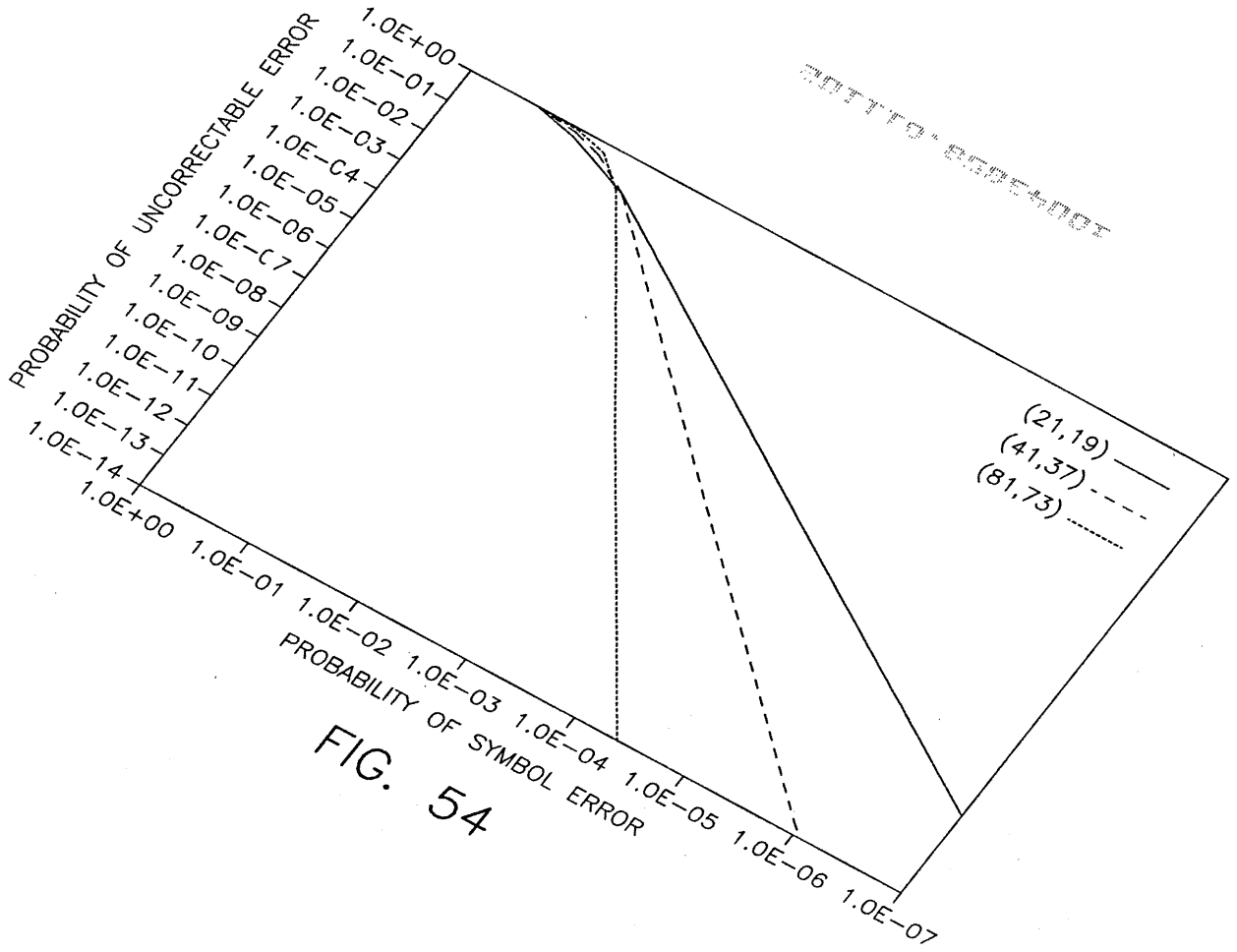

PROBABILITY OF UNCORRECTABLE ERROR
1.0E+00
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
1.0E-13
1.0E-14
1.0E+00 1.0E-01 1.0E-02 1.0E-03 1.0E-04 1.0E-05 1.0E-06 1.0E-07
PROBABILITY OF SYMBOL ERROR
(21,19)
(41,37)
(81,73)

FIG. 54

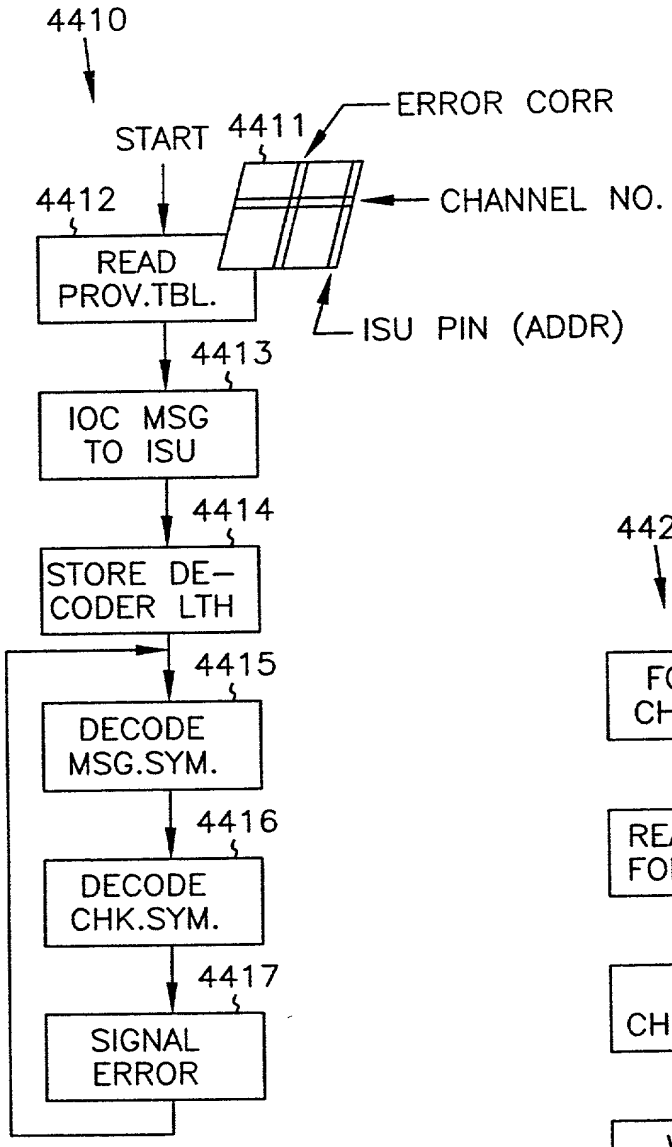

4410
START
4411
ERROR CORR
4412
CHANNEL NO.
READ PROV.TBL.
ISU PIN (ADDR)
4413
IOC MSG TO ISU
4414
STORE DE-CODER LTH
4415
DECODE MSG.SYM.
4416
DECODE CHK.SYM.
4417
SIGNAL ERROR

FIG. 55

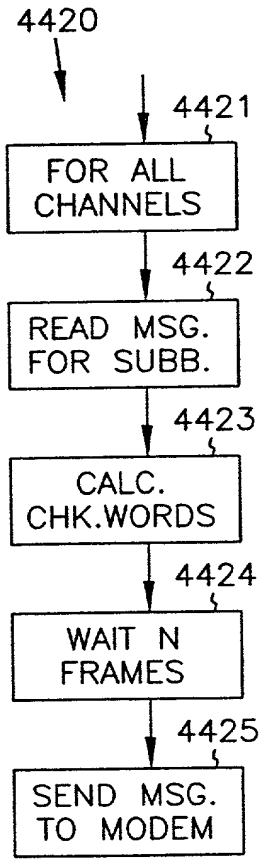

4420
4421
FOR ALL CHANNELS
4422
READ MSG. FOR SUBB.
4423
CALC. CHK.WORDS
4424
WAIT N FRAMES
4425
SEND MSG. TO MODEM

FIG. 56

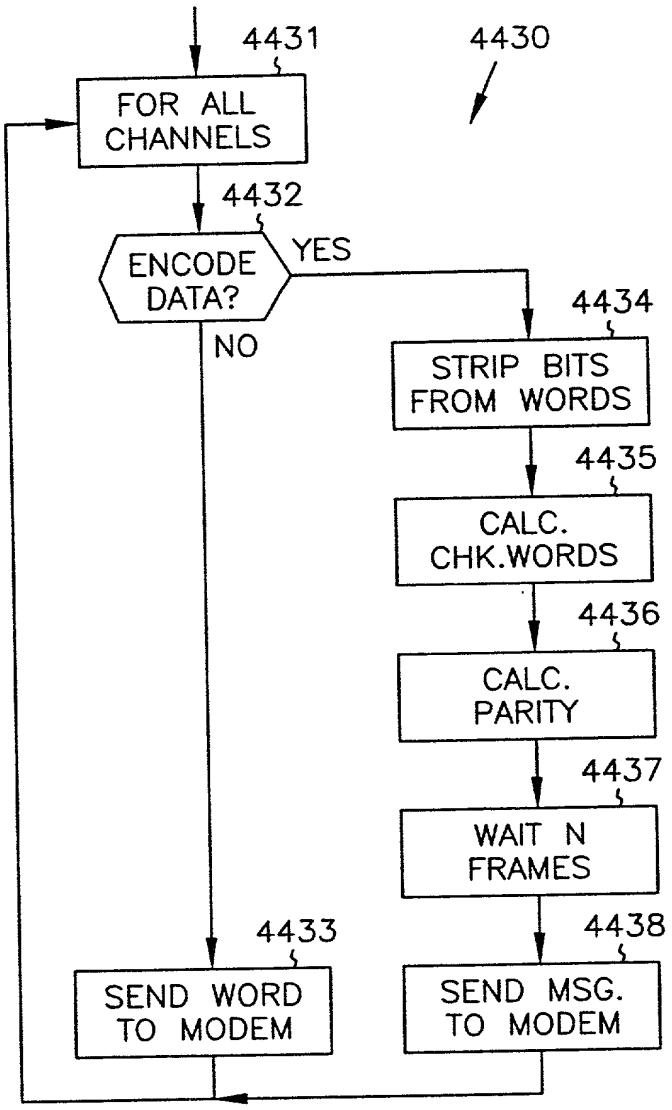

4431
4430
FOR ALL CHANNELS
4432
ENCODE DATA?
YES
NO
4434
STRIP BITS FROM WORDS
4435
CALC. CHK.WORDS
4436
CALC. PARITY
4437
WAIT N FRAMES
4433
SEND WORD TO MODEM
4438
SEND MSG. TO MODEM

FIG. 57

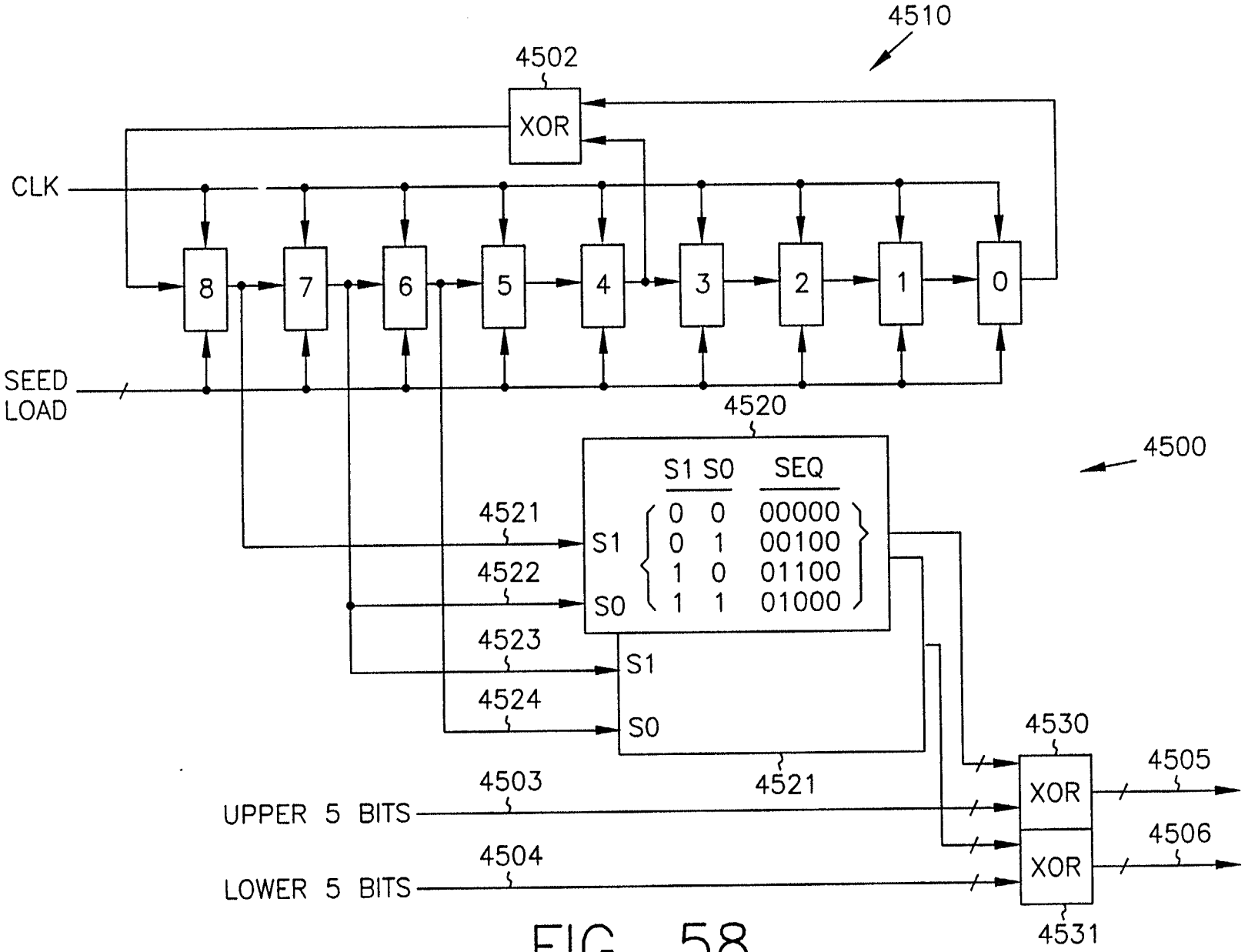


FIG. 58

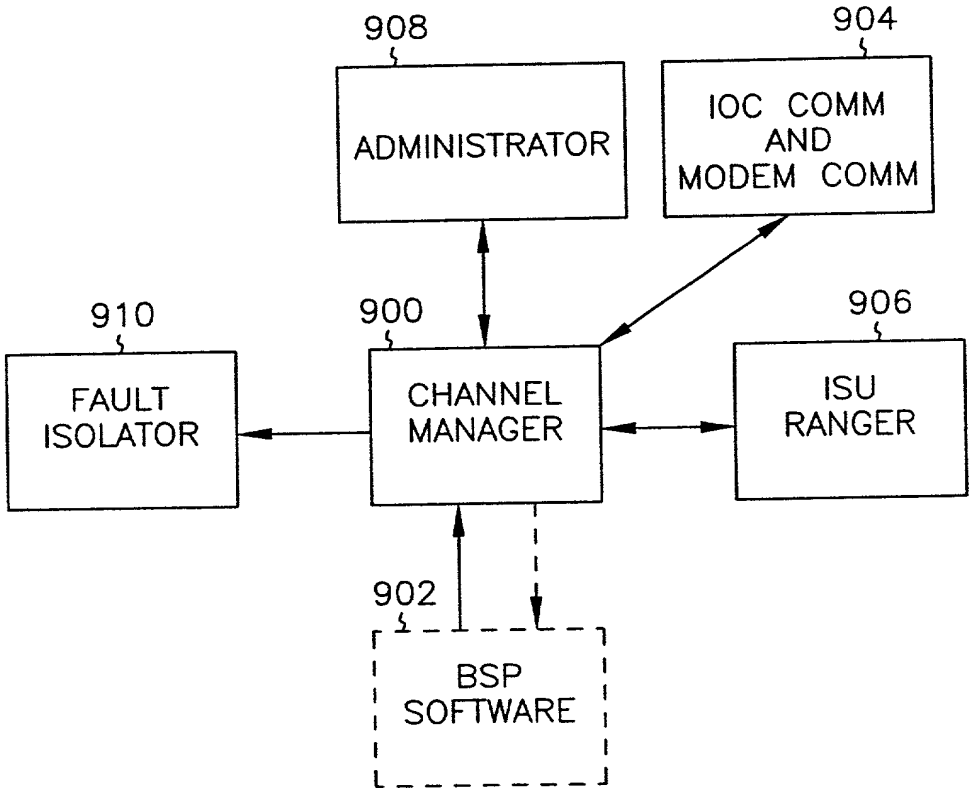

908
ADMINISTRATOR
904
IOC COMM AND MODEM COMM
910
FAULT ISOLATOR
900
CHANNEL MANAGER
906
ISU RANGER
902
BSP SOFTWARE

FIG. 59

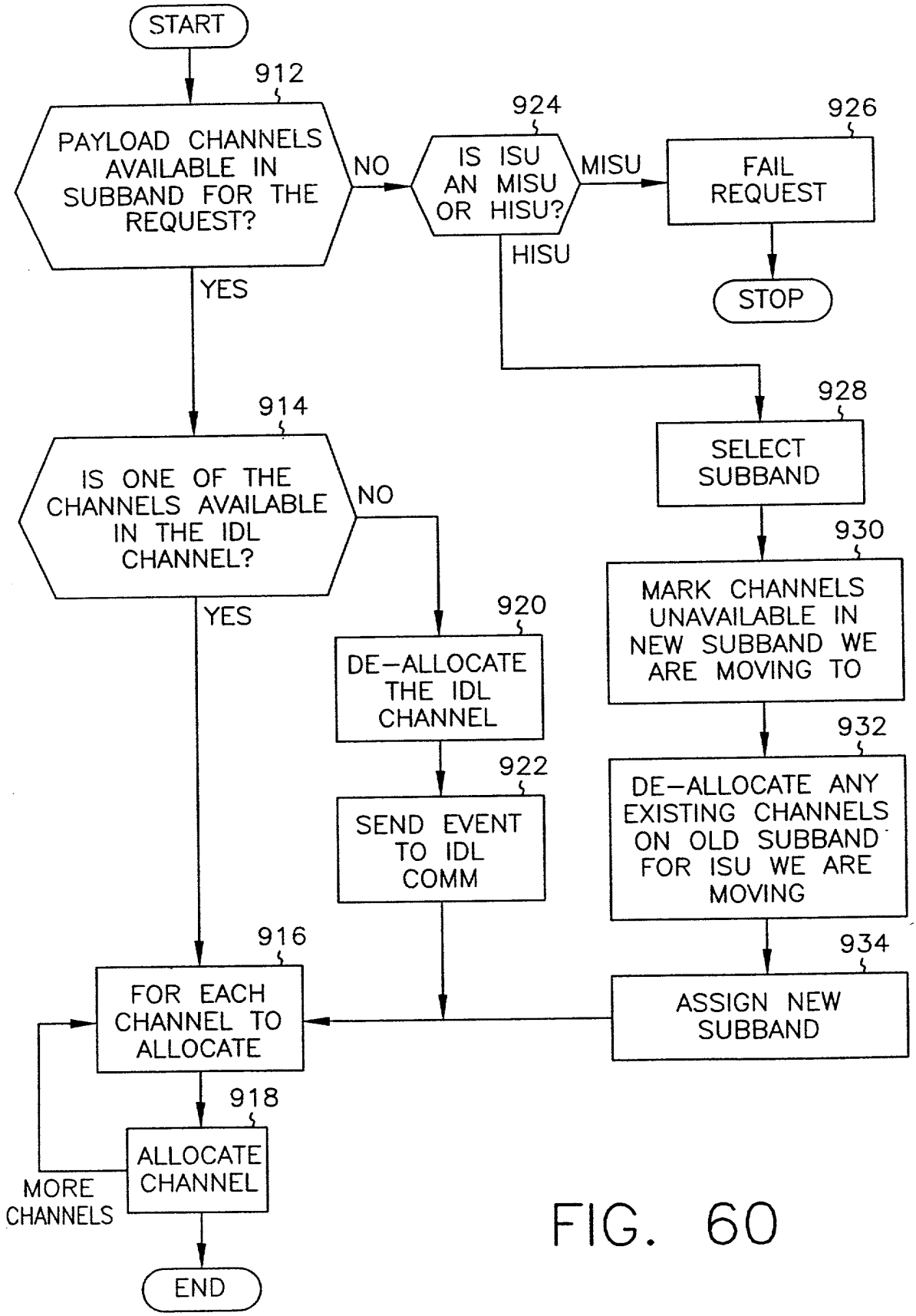

START
912
PAYLOAD CHANNELS AVAILABLE IN SUBBAND FOR THE REQUEST?
NO
924
IS ISU AN MISU OR HISU?
MISU
926
FAIL REQUEST
STOP
HISU
YES
914
IS ONE OF THE CHANNELS AVAILABLE IN THE IDL CHANNEL?
NO
YES
920
DE-ALLOCATE THE IDL CHANNEL
922
SEND EVENT TO IDL COMM
928
SELECT SUBBAND
930
MARK CHANNELS UNAVAILABLE IN NEW SUBBAND WE ARE MOVING TO
932
DE-ALLOCATE ANY EXISTING CHANNELS ON OLD SUBBAND FOR ISU WE ARE MOVING
934
ASSIGN NEW SUBBAND
916
FOR EACH CHANNEL TO ALLOCATE
918
ALLOCATE CHANNEL
MORE CHANNELS
END

FIG. 60

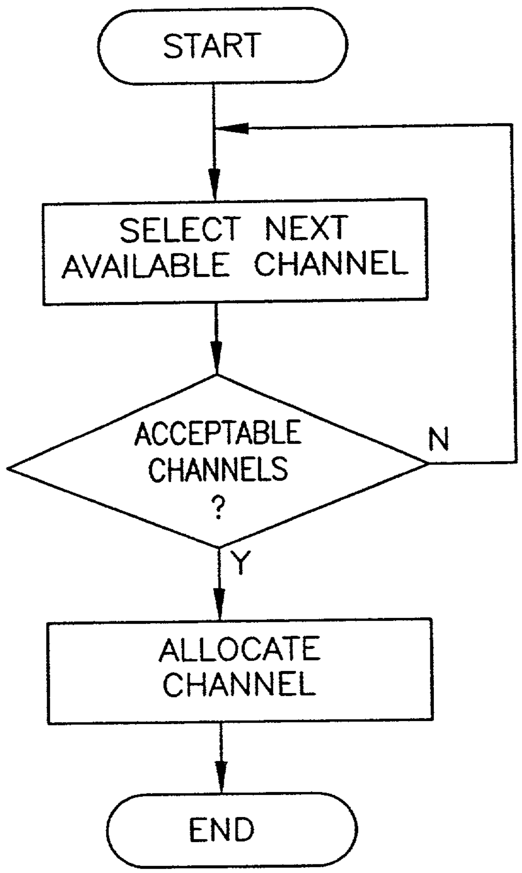

START
SELECT NEXT AVAILABLE CHANNEL
ACCEPTABLE CHANNELS ?
N
Y
ALLOCATE CHANNEL
END

FIG. 61

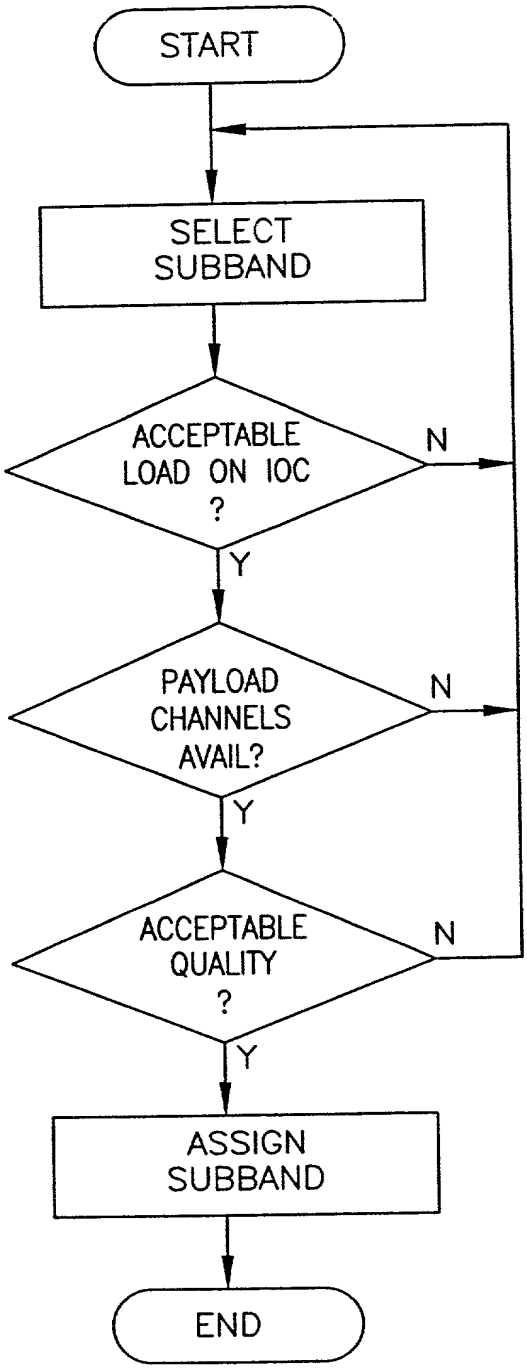

START
SELECT SUBBAND
ACCEPTABLE LOAD ON IOC ?
N
Y
PAYLOAD CHANNELS AVAIL?
N
Y
ACCEPTABLE QUALITY ?
N
Y
ASSIGN SUBBAND
END

FIG. 62

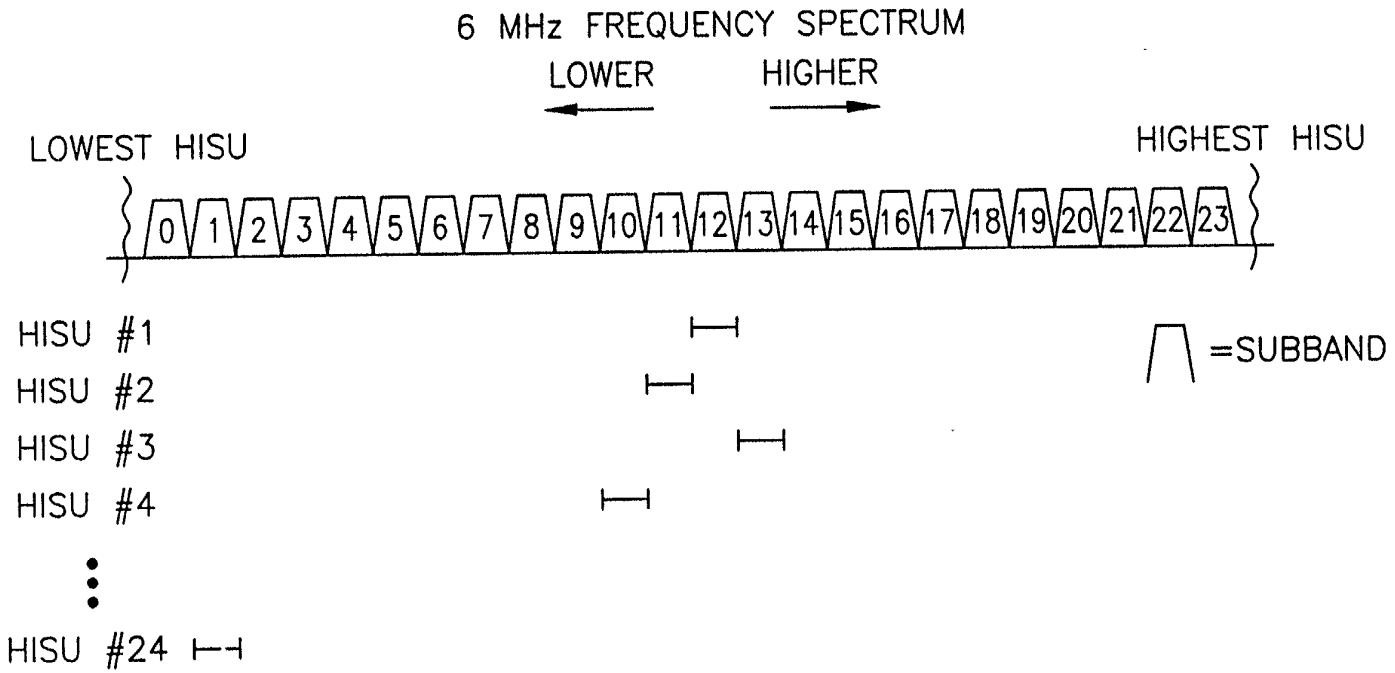

6 MHz FREQUENCY SPECTRUM
LOWER
HIGHER
LOWEST HISU
HIGHEST HISU
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
HISU #1
HISU #2
HISU #3
HISU #4
HISU #24
=SUBBAND

FIG. 63

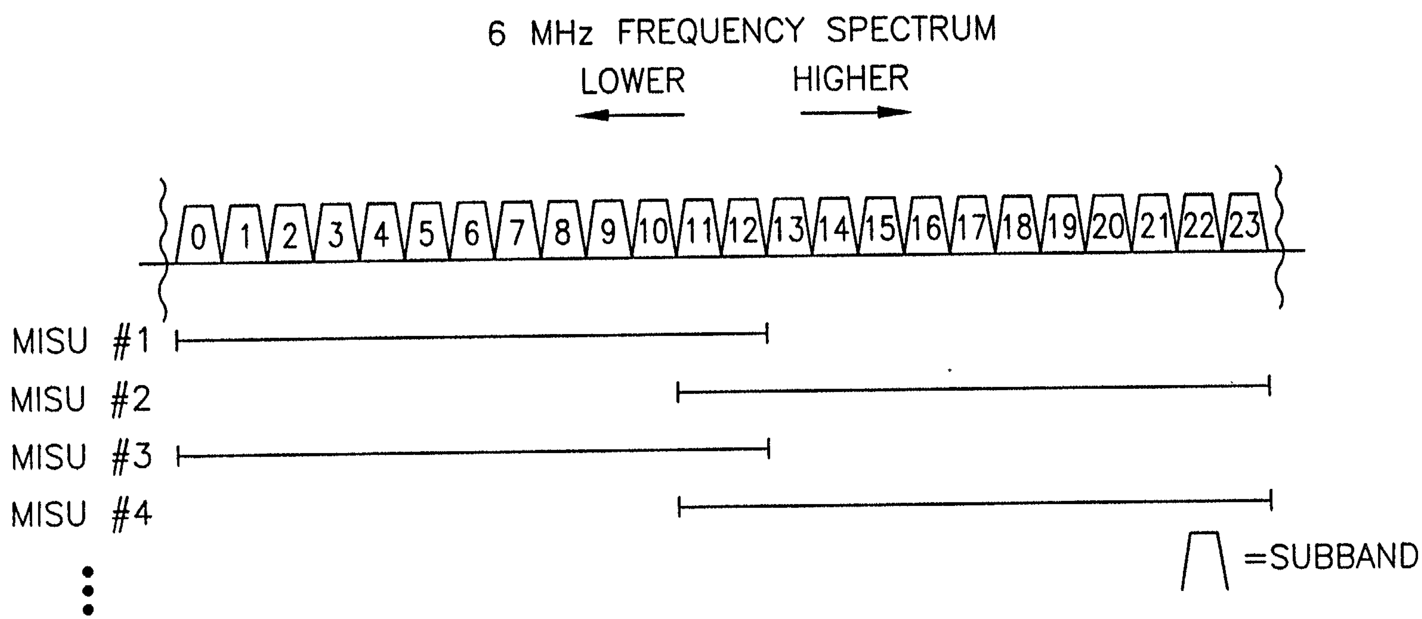


FIG. 64

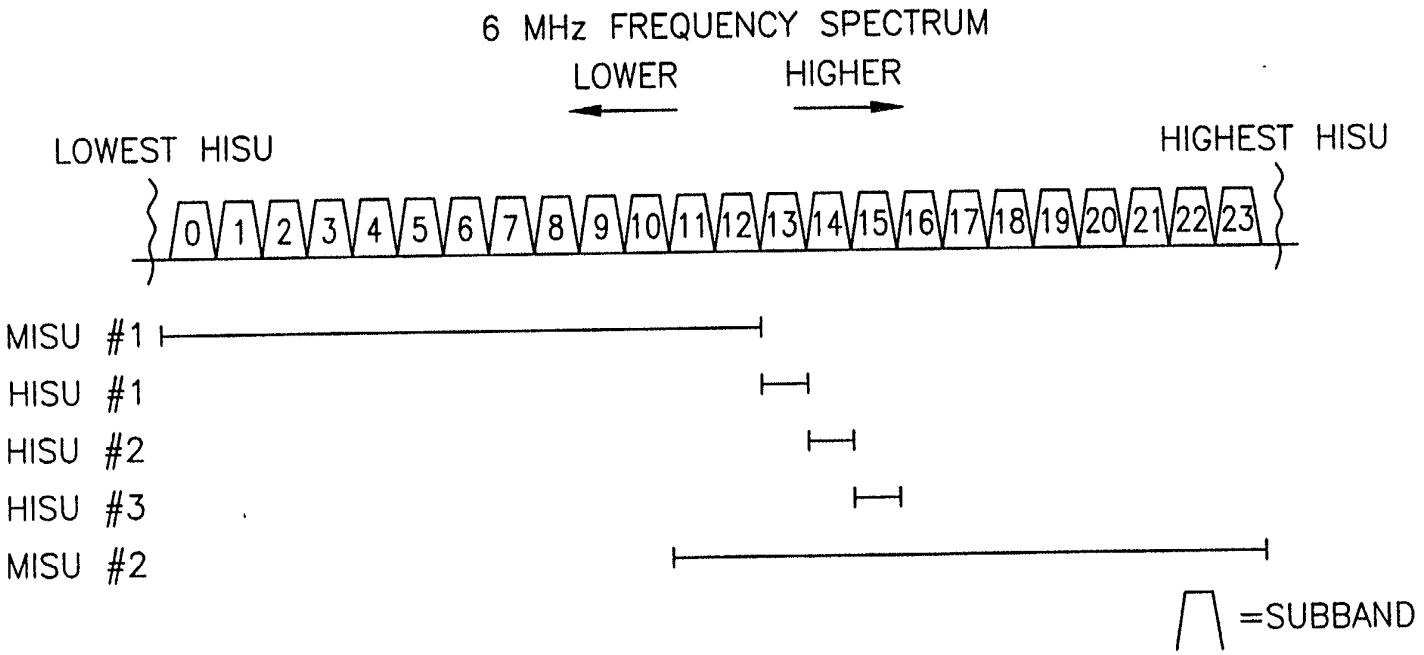

6 MHz FREQUENCY SPECTRUM
LOWER
HIGHER
LOWEST HISU
HIGHEST HISU
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
MISU #1
HISU #1
HISU #2
HISU #3
MISU #2
=SUBBAND

FIG. 65

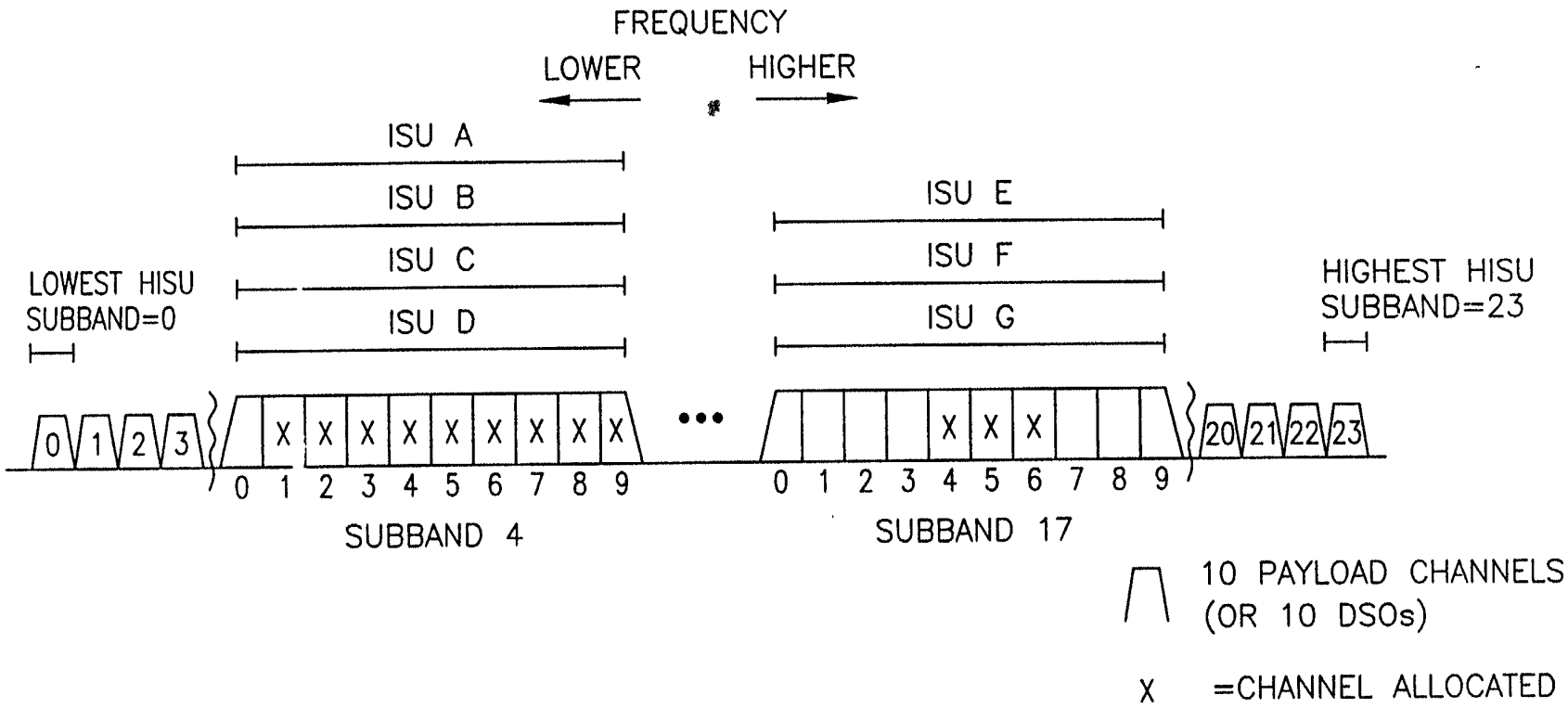


FIG. 66

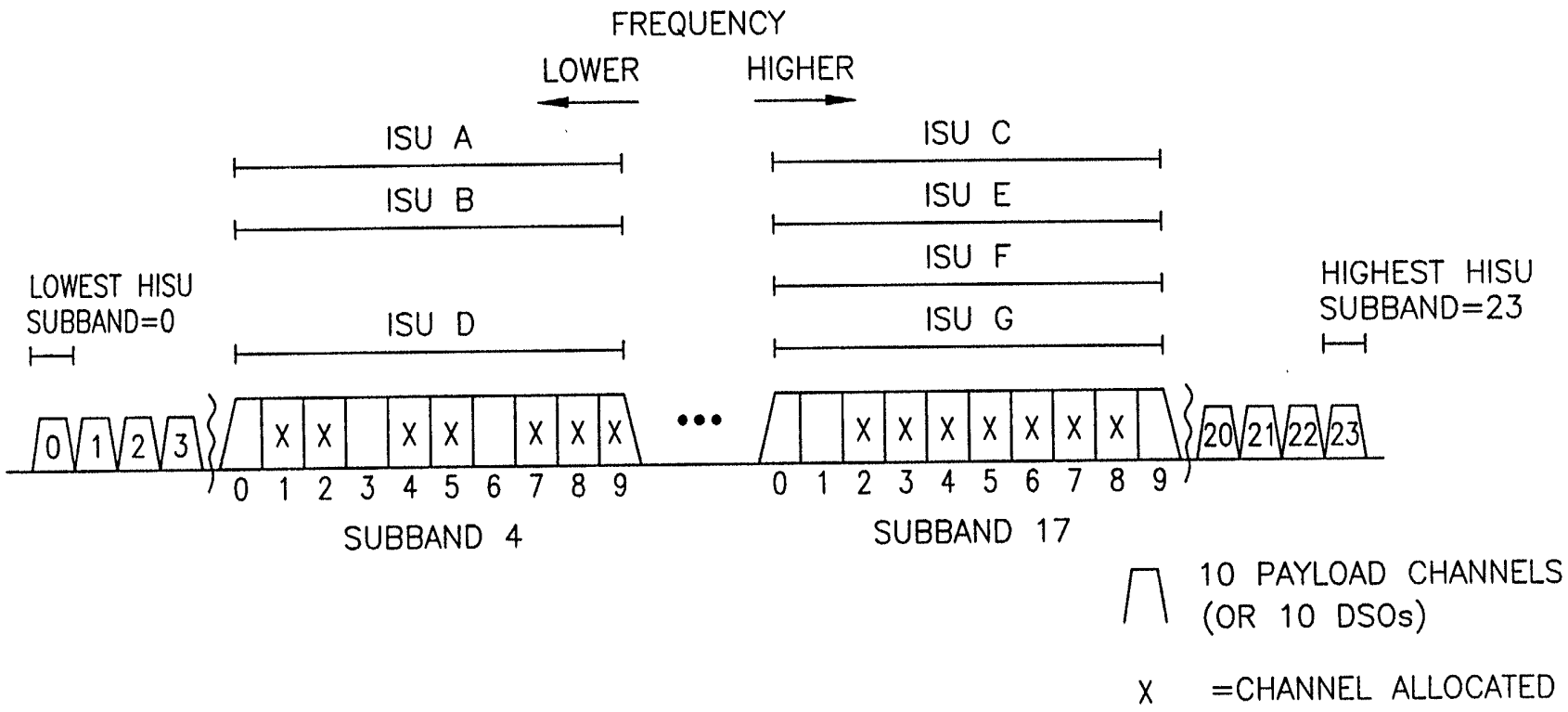

FREQUENCY
LOWER
HIGHER
ISU A
ISU B
ISU C
ISU E
ISU F
ISU G
ISU D
LOWEST HISU
SUBBAND=0
HIGHEST HISU
SUBBAND=23
0 1 2 3
X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 4
X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 17
20 21 22 23
10 PAYLOAD CHANNELS
(OR 10 DSOs)
X =CHANNEL ALLOCATED

FIG. 67

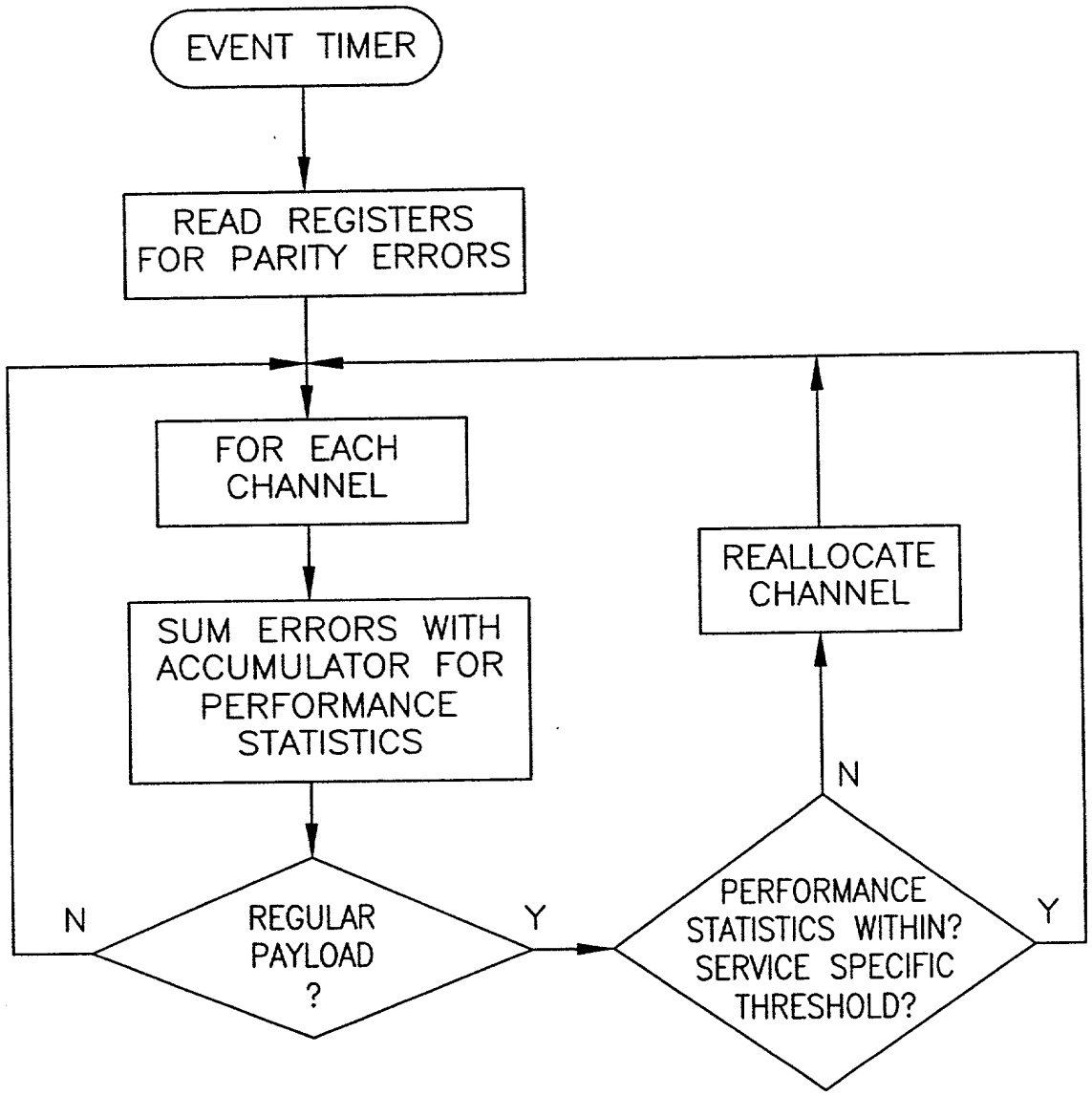

EVENT TIMER
READ REGISTERS FOR PARITY ERRORS
FOR EACH CHANNEL
SUM ERRORS WITH ACCUMULATOR FOR PERFORMANCE STATISTICS
REGULAR PAYLOAD ?
N
Y
PERFORMANCE STATISTICS WITHIN? SERVICE SPECIFIC THRESHOLD?
N
Y
REALLOCATE CHANNEL

FIG. 68

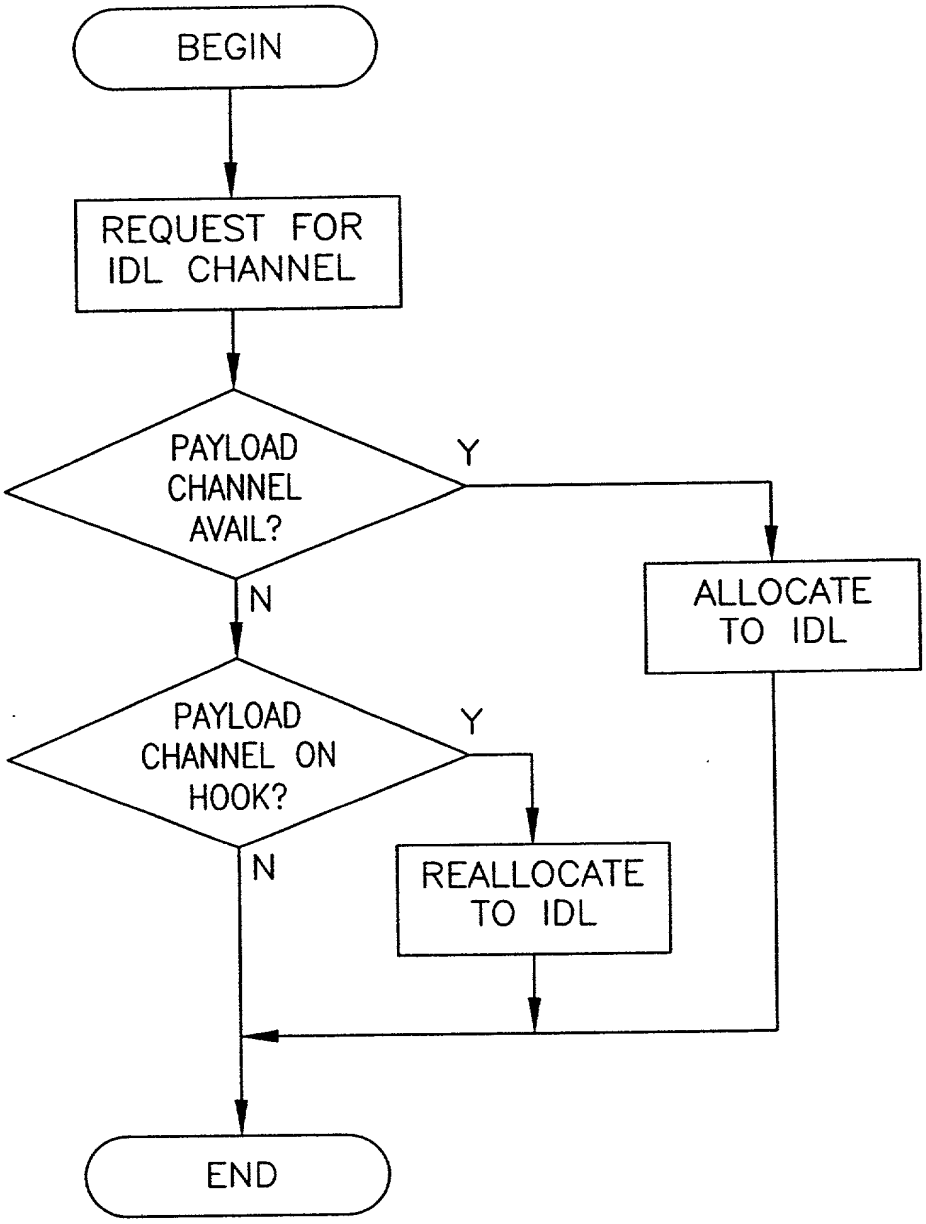

BEGIN
REQUEST FOR IDL CHANNEL
PAYLOAD CHANNEL AVAIL?
Y
N
ALLOCATE TO IDL
PAYLOAD CHANNEL ON HOOK?
Y
N
REALLOCATE TO IDL
END

FIG. 69

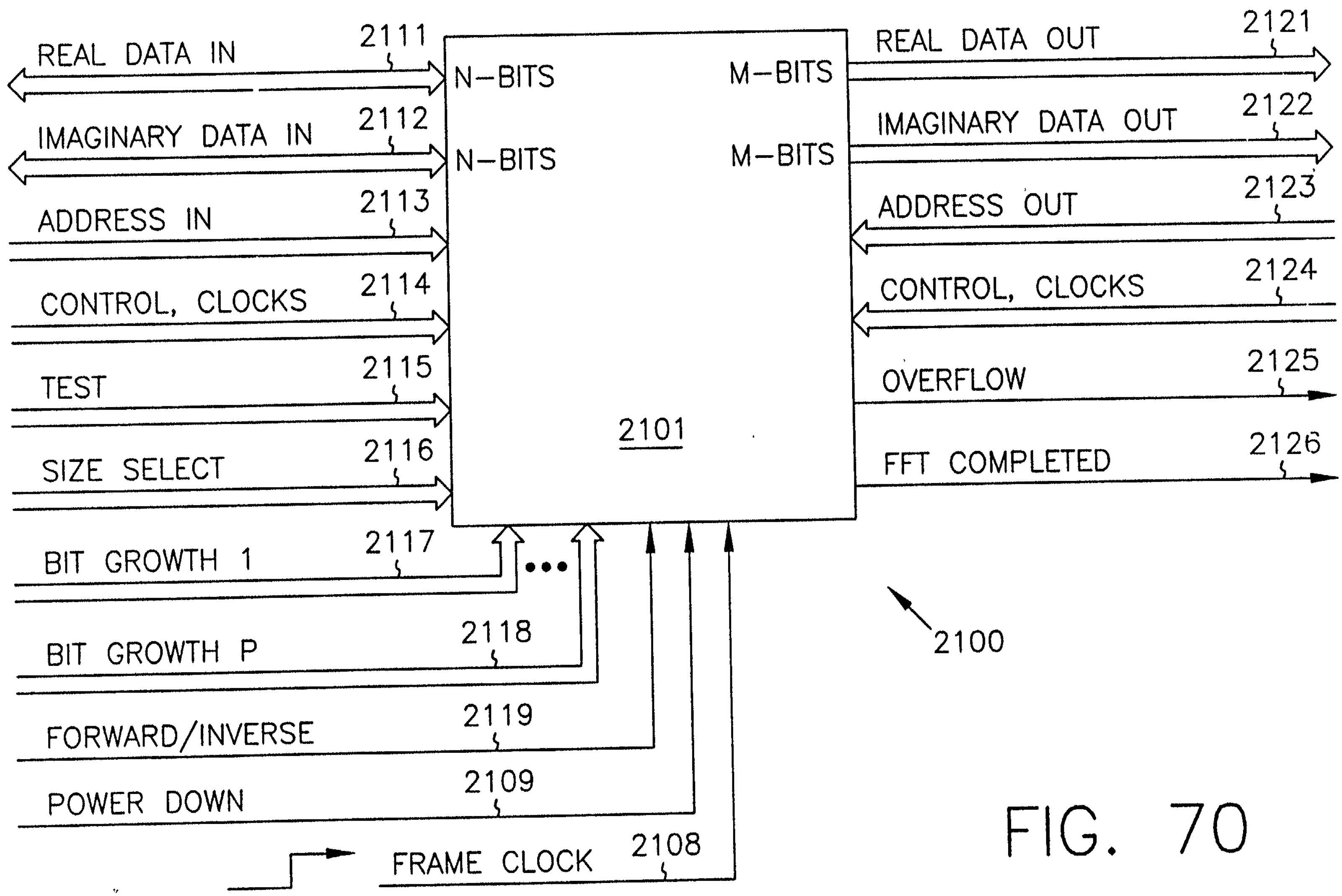

REAL DATA IN
2111
IMAGINARY DATA IN
2112
ADDRESS IN
2113
CONTROL, CLOCKS
2114
TEST
2115
SIZE SELECT
2116
BIT GROWTH 1
2117
BIT GROWTH P
2118
FORWARD/INVERSE
2119
POWER DOWN
2109
FRAME CLOCK
2108
N-BITS
N-BITS
M-BITS
M-BITS
2101
REAL DATA OUT
2121
IMAGINARY DATA OUT
2122
ADDRESS OUT
2123
CONTROL, CLOCKS
2124
OVERFLOW
2125
FFT COMPLETED
2126
2100

FIG. 70

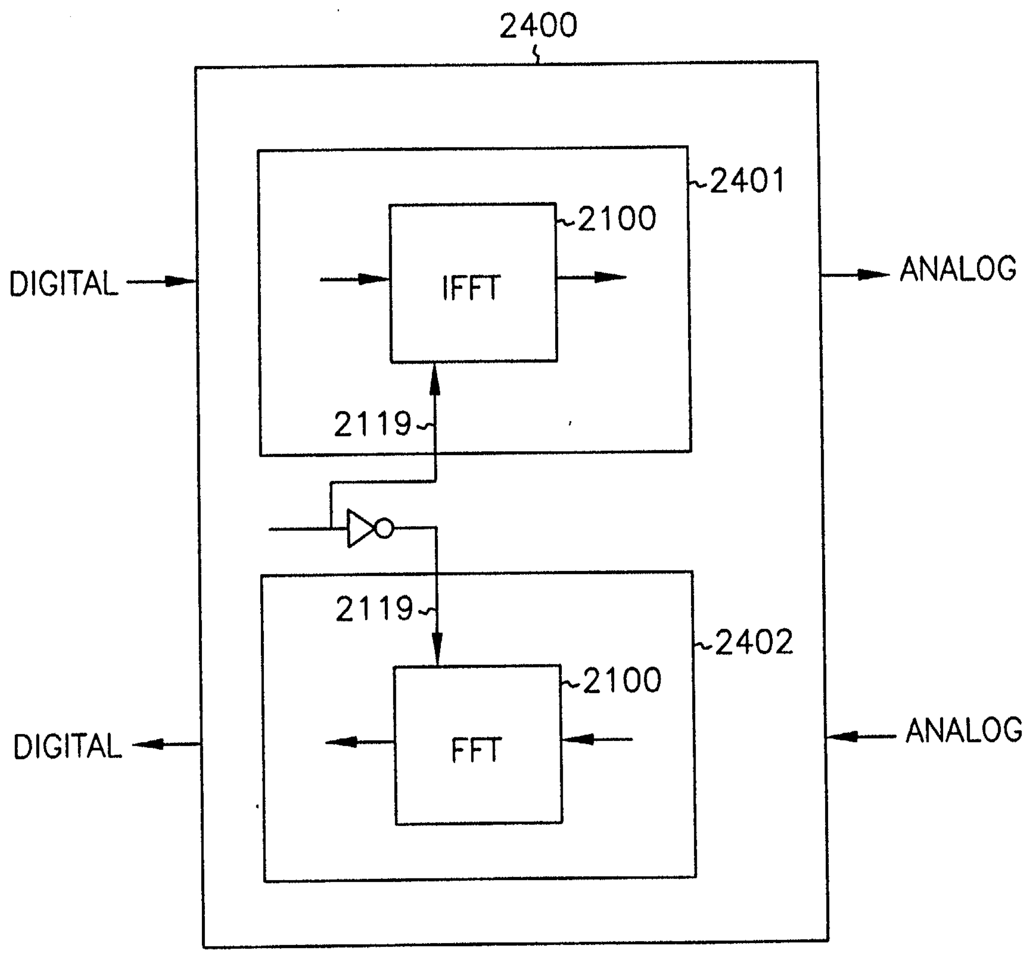

2400
2401
2100
DIGITAL
IFFT
ANALOG
2119
2119
2402
2100
DIGITAL
FFT
ANALOG

FIG. 71

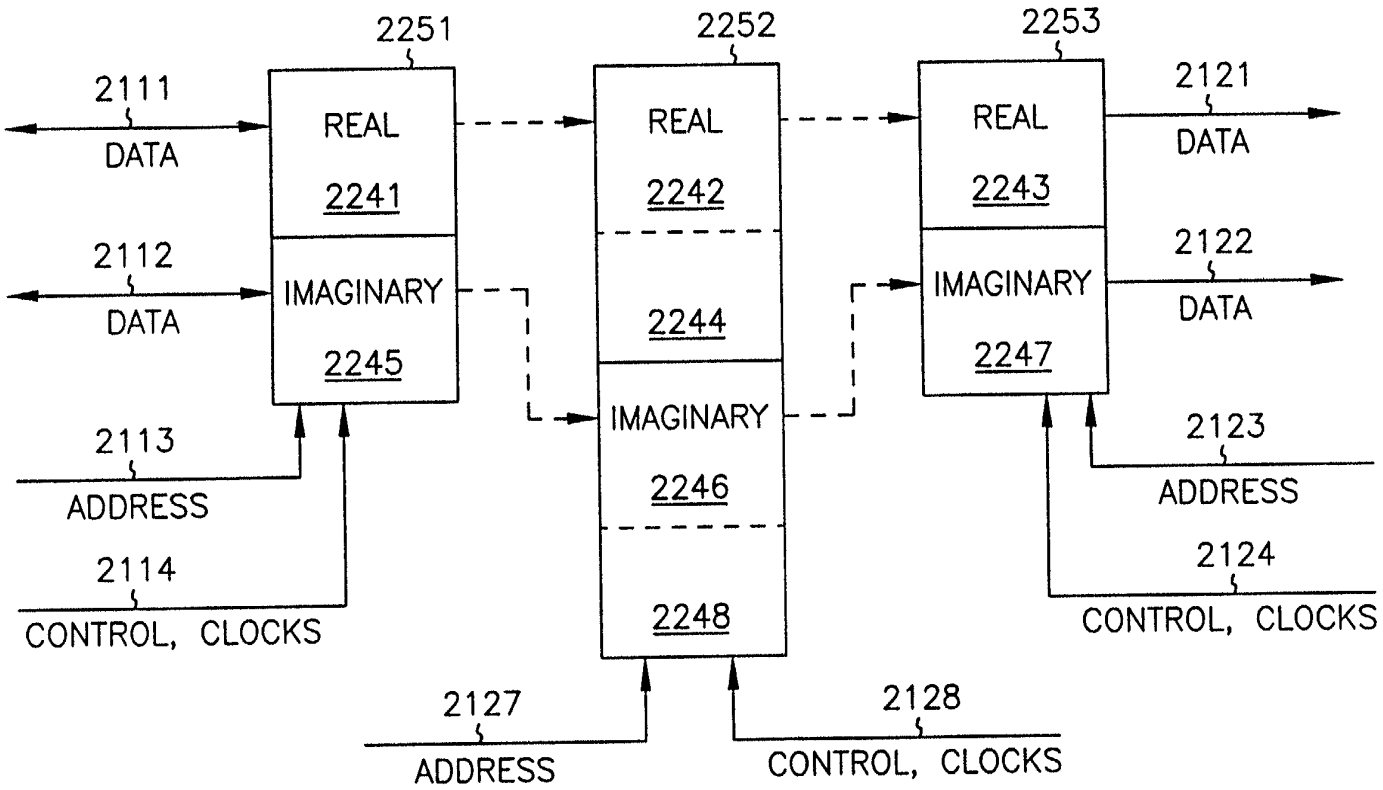

2251
2252
2253
2111
DATA
REAL
2241
REAL
2242
REAL
2243
2121
DATA
2112
DATA
IMAGINARY
2245
2244
IMAGINARY
2247
2122
DATA
IMAGINARY
2246
2113
ADDRESS
2123
ADDRESS
2114
CONTROL, CLOCKS
2248
2124
CONTROL, CLOCKS
2127
ADDRESS
2128
CONTROL, CLOCKS

FIG. 72

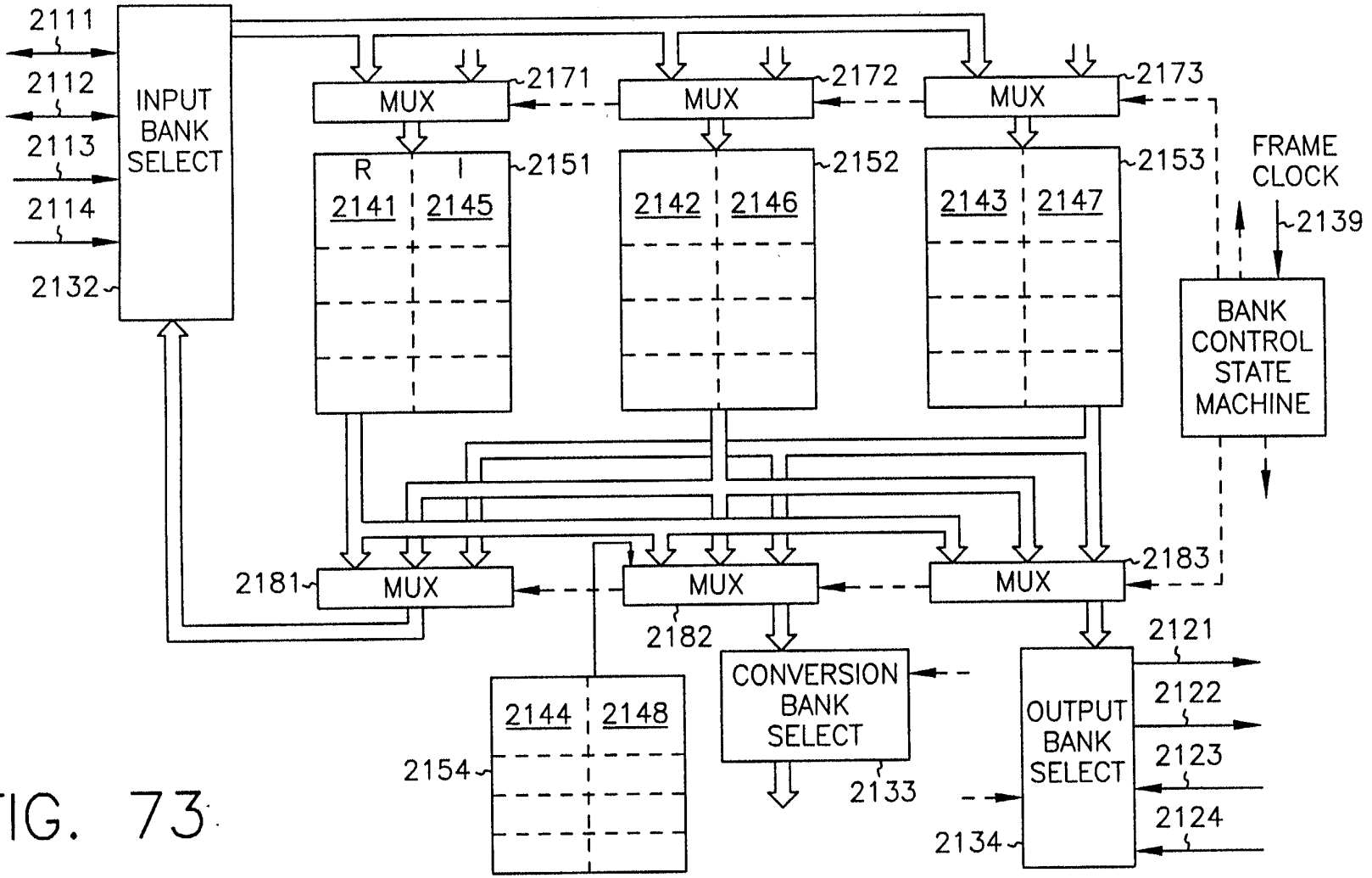
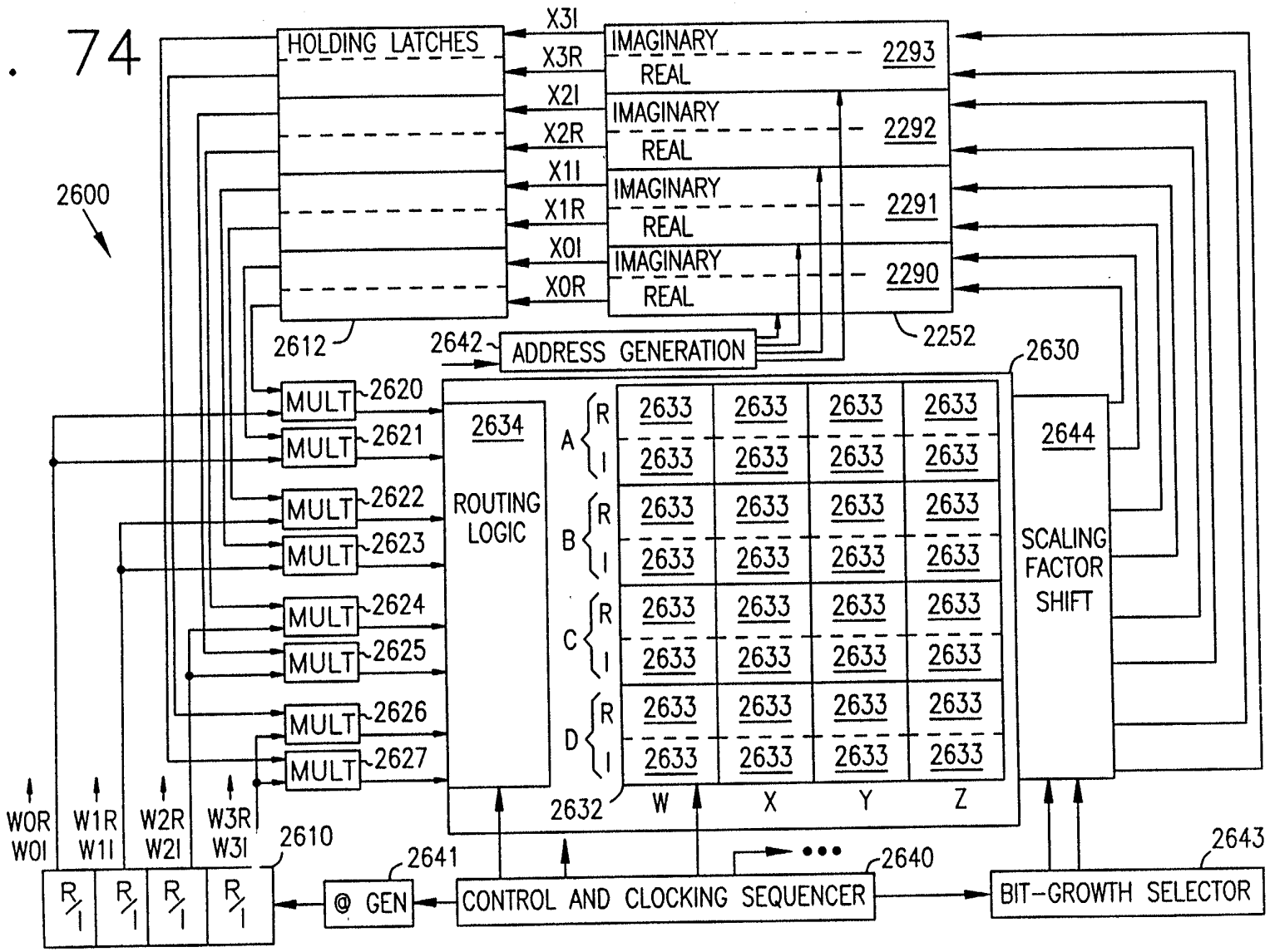

2111
2112
2113
2114
2132
INPUT BANK SELECT
MUX
2171
MUX
2172
MUX
2173
R
I
2141
2145
2151
2142
2146
2152
2143
2147
2153
FRAME CLOCK
2139
BANK CONTROL STATE MACHINE
2181
MUX
MUX
MUX
2183
2182
2121
2122
2123
2124
CONVERSION BANK SELECT
2133
OUTPUT BANK SELECT
2134
2144
2148
2154

FIG. 73

FIG. 74


2600
HOLDING LATCHES
X3I
X3R
X2I
X2R
X1I
X1R
X0I
X0R
IMAGINARY
REAL
2293
2292
2291
2290
2612
2642
ADDRESS GENERATION
2252
2630
MULT
2620
2621
2622
2623
2624
2625
2626
2627
2634
ROUTING LOGIC
A
B
C
D
R
I
2633
2644
SCALING FACTOR SHIFT
W
X
Y
Z
2632
W0R
W0I
W1R
W1I
W2R
W2I
W3R
W3I
2610
R/I
@ GEN
2641
CONTROL AND CLOCKING SEQUENCER
2640
BIT-GROWTH SELECTOR
2643

THIS TABLE SHOWS THE ORDER OF CALCULATION FOR A TRANSPOSED BUTTERFLY:

C0

AWR=WR AWI =WI	AXR =XR AXI =XI	AYR =YR AYI =YI	AZR =ZR AZI =ZI
BWR=WR BWI =WI	BXR=XR BXI =XI	BYR =YR BYI =YI	BZR=ZR BZI =ZI
CWR=WR CWI =WI	CXR=XR CXI =XI	CYR =YR CYI =YI	CZR=ZR CZI =ZI
DWR=WR DWI =WI	DXR=XR DXI =XI	DYR =YR DYI =YI	DZR=ZR DZI =ZI

~2632

2800

FIG. 75

CI

AWR=AWR −WI AWI=AWI +WR	AXR=AXR −XI AXI=AXI +XR	AYR=AYR −YI AYI=AYI +YR	AZR=AZR −ZI AZI=AZI +ZR
BWR=BWR−WI BWI=BWI +WR	BXR=BXR −XI BXI=BXI +XR	BYR=BYR −YI BYI=BYI +YR	BZR=BZR −ZI BZI=BZI +ZR
CWR=CWR−WI CWI=CWI +WR	CXR=CXR −XI CXI=CXI +XR	CYR=CYR −YI CYI=CYI +YR	CZR=CZR −ZI CZI=CZI +ZR
DWR=DWR−WI DWI=DWI +WR	DXR=DXR −XI DXI=DXI +XR	DYR=DYR −YI DYI=DYI +YR	DZR=DZR −ZI DZI=DZI +ZR

~2632

2800

FIG. 76

C2

AWR=AWR +WR AWI=AWI +WI	AXR=AXR +XI AXI=AXI −XR	AYR=AYR −YR AYI=AYI −YI	AZR=AZR −ZI AZI=AZI +ZR
BWR=BWR+WR BWI=BWI +WI	BXR=BXR +XI BXI=BXI −XR	BYR=BYR −YR BYI=BYI −YI	BZR=BZR −ZI BZI=BZI +ZR
CWR=CWR+WR CWI=CWI +WI	CXR=CXR +XI CXI=CXI −XR	CYR=CYR −YR CYI=CYI −YI	CZR=CZR −ZI CZI=CZI +ZR
DWR=DWR+WR DWI=DWI +WI	DXR=DXR +XI DXI=DXI −XR	DYR=DYR −YR DYI=DYI −YI	DZR=DZR −ZI DZI=DZI +ZR

2632

2800

FIG. 77

C3

AWR=AWR −WI AWI=AWI +WR	AXR=AXR +XR AXI=AXI +XI	AYR=AYR +YI AYI=AYI −YR	AZR=AZR −ZR AZI=AZI −ZI
BWR=BWR−WI BWI=BWI +WR	BXR=BXR +XR BXI=BXI +XI	BYR=BYR +YI BYI=BYI −YR	BZR=BZR −ZR BZI=BZI −ZI
CWR=CWR−WI CWI=CWI +WR	CXR=CXR +XR CXI=CXI +XI	CYR=CYR +YI CYI=CYI −YR	CZR=CZR −ZR CZI=CZI −ZI
DWR=DWR−WI DWI=DWI +WR	DXR=DXR +XR DXI=DXI +XI	DYR=DYR +YI DYI=DYI −YR	DZR=DZR −ZR DZI=DZI −ZI

2632

2800

FIG. 78

C4

AWR=AWR +WR AWI=AWI +WI	AXR=AXR −XR AXI=AXI −XI	AYR=AYR +YR AYI=AYI +YI	AZR=AZR −ZR AZI=AZI −ZI
BWR=BWR+WR BWI=BWI +WI	BXR=BXR −XR BXI=BXI −XI	BYR=BYR +YR BYI=BYI +YI	BZR=BZR −ZR BZI=BZI −ZI
CWR=CWR+WR CWI=CWI +WI	CXR=CXR −XR CXI=CXI −XI	CYR=CYR +YR CYI=CYI +YI	CZR=CZR −ZR CZI=CZI −ZI
DWR=DWR+WR DWI=DWI +WI	DXR=DXR −XR DXI=DXI −XI	DYR=DYR +YR DYI=DYI +YI	DZR=DZR −ZR DZI=DZI −ZI

~2632

2800

FIG. 79

C5

AWR=AWR −WI AWI=AWI +WR	AXR=AXR +XI AXI=AXI −XR	AYR=AYR −YI AYI=AYI +YR	AZR=AZR +ZI AZI=AZI −ZR
BWR=BWR−WI BWI=BWI +WR	BXR=BXR +XI BXI=BXI −XR	BYR=BYR −YI BYI=BYI +YR	BZR=BZR +ZI BZI=BZI −ZR
CWR=CWR−WI CWI=CWI +WR	CXR=CXR +XI CXI=CXI −XR	CYR=CYR −YI CYI=CYI +YR	CZR=CZR +ZI CZI=CZI −ZR
DWR=DWR−WI DWI=DWI +WR	DXR=DXR +XI DXI=DXI −XR	DYR=DYR −YI DYI=DYI +YR	DZR=DZR +ZI DZI=DZI −ZR

~2632

2800

FIG. 80

C6

AWR=AWR +WR AWI=AWI +WI	AXR=AXR −XI AXI=AXI +XR	AYR=AYR −YR AYI=AYI −YI	AZR=AZR +ZI AZI=AZI −ZR
BWR=BWR+WR BWI=BWI +WI	BXR=BXR −XI BXI=BXI +XR	BYR=BYR −YR BYI=BYI −YI	BZR=BZR +ZI BZI=BZI −ZR
CWR=CWR+WR CWI=CWI +WI	CXR=CXR −XI CXI=CXI +XR	CYR=CYR −YR CYI=CYI −YI	CZR=CZR +ZI CZI=CZI −ZR
DWR=DWR+WR DWI=DWI +WI	DXR=DXR −XI DXI=DXI +XR	DYR=DYR −YR DYI=DYI −YI	DZR=DZR +ZI DZI=DZI −ZR

2632

2800

FIG. 81

C7

AWR=A VR −WI AWI=AWI +WR	AXR=AXR −XR AXI=AXI −XI	AYR=AYR +YI AYI=AYI −YR	AZR=AZR −ZR AZI=AZI +ZI
BWR=BWR−WI BWI=BWI +WR	BXR=BXR −XR BXI=BXI −XI	BYR=BYR +YI BYI=BYI −YR	BZR=BZR −ZR BZI=BZI +ZI
CWR=CWR−WI CWI=CWI +WR	CXR=CXR −XR CXI=CXI −XI	CYR=CYR +YI CYI=CYI −YR	CZR=CZR −ZR CZI=CZI +ZI
DWR=DWR−WI DWI=DWI +WR	DXR=DXR −XR DXI=DXI −XI	DYR=DYR +YI DYI=DYI −YR	DZR=DZR −ZR DZI=DZI +ZI

2632

2800

FIG. 82

THIS TABLE SHOWS THE ORDER OF CALCULATION FOR A TRANSPOSED BUTTERFLY:

C0 (2632, 2810)

AWR =WR+XR+YR+ZR AWI =WI+XI+YI+ZI	AXR =WR−XI−YR+ZI AXI =WI+XR−YI−ZR	AYR =WR−XR+YR−ZR AYI =WI−XI+YI−ZI	AZR =WR+XI−YR−ZI AZI =WI−XR−YI+ZR
– –	– –	– –	– –
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 83

C1 (2632, 2810)

AWR =AWR−(WI+XI+YI+ZI) AWI =AWI+(WR+XR+YR+ZR)	AXR =AXR−(WI+XR−YI−ZR) AXI =AXI+(WR−XI−YR+ZI)	AYR =AYR−(WI−XI+YI−ZI) AYI =AYI+(WR−XR+YR−ZR)	AZR =AZR−(WI−XR−YI+ZR) AZI =AZI+(WR+XI−YR−ZI)
– –	– –	– –	– –
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 84

C2

2632

2810

– –	– –	– –	– –
BWR =WR+XR+YR+ZR BWI =WI+XI+YI+ZI	BXR =WR−XI−YR+ZI BXI =WI+XR−YI−ZR	BYR =WR−XR+YR−ZR BYI =WI−XI+YI−ZI	BZR =WR+XI−YR−ZI BZI =WI−XR−YI+ZR
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 85

C3

2632

2810

– –	– –	– –	– –
BWR =BWR−(WI+XI+YI+ZI) BWI =BWI+(WR+XR+YR+ZR)	BXR =BXR−(WI+XR−YI−ZR) BXI =BXI+(WR−XI−YR+ZI)	BYR =BYR−(WI−XI+YI−ZI) BYI =BYI+(WR−XR+YR−ZR)	BZR =BZR−(WI−XR−YI+ZR) BZI =BZI+(WR+XI−YR−ZI)
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 86

C4

2632

2810

–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
CWR =WR+XR+YR+ZR CWI =WI+XI+YI+ZI	CXR =WR−XI−YR+ZI CXI =WI+XR−YI−ZR	CYR =WR−XR+YR−ZR CYI =WI−XI+YI−ZI	CZR =WR+XI−YR−ZI CZI =WI−XR−YI+ZR
–	–	–	–
–	–	–	–

FIG. 87

C5

2632

2810

–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
CWR =CWR−(WI+XI+YI+ZI) CWI =CWI+(WR+XR+YR+ZR)	CXR =CXR−(WI+XR−YI−ZR) CXI =CXI+(WR−XI−YR+ZI)	CYR =CYR−(WI−XI+YI−ZI) CYI =CYI+(WR−XR+YR−ZR)	CZR =CZR−(WI−XR−YI+ZR) CZI =CZI+(WR+XI−YR−ZI)
–	–	–	–
–	–	–	–

FIG. 88

C6 2632 2810

– –	– –	– –	– –
– –	– –	– –	– –
– –	– –	– –	– –
DWR =WR+XR+YR+ZR DWI =WI+XI+YI+ZI	DXR =WR−XI−YR+ZI DXI =WI+XR−YI−ZR	DYR =WR−XR+YR−ZR DYI =WI−XI+YI−ZI	DZR =WR+XI−YR−ZI DZI =WI−XR−YI+ZR

FIG. 89

C7 2632 2810

– –	– –	– –	– –
– –	– –	– –	– –
– –	– –	– –	– –
DWR =DWR−(WI+XI+YI+ZI) DWI =DWI+(WR+XR+YR+ZR)	DXR =DXR−(WI+XR−YI−ZR) DXI =DXI+(WR−XI−YR+ZI)	DYR =DYR−(WI−XI+YI−ZI) DYI =DYI+(WR−XR+YR−ZR)	DZR =DZR−(WI−XR−YI+ZR) DZI =DZI+(WR+XI−YR−ZI)

FIG. 90

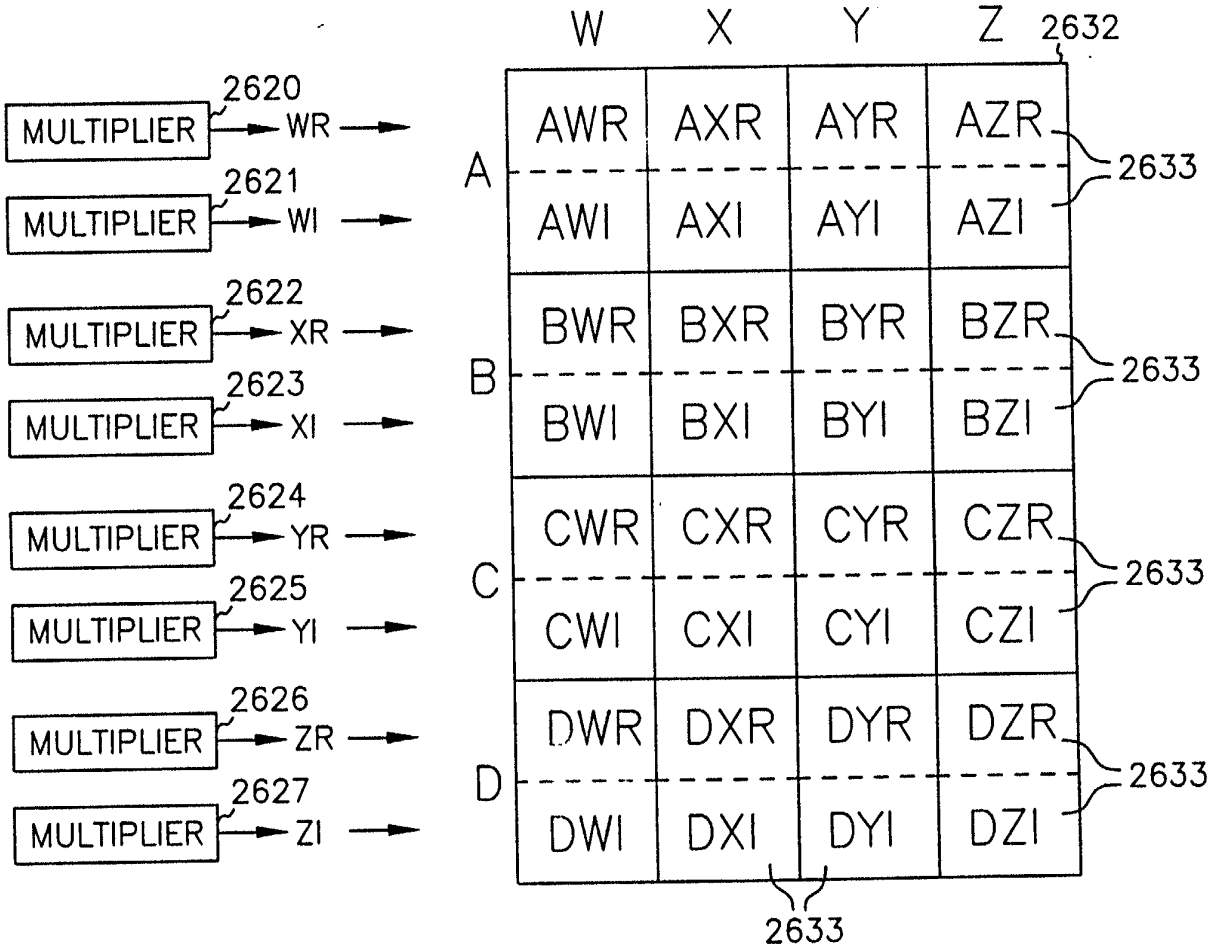

W
X
Y
Z
2632
MULTIPLIER
2620
WR
2621
WI
2622
XR
2623
XI
2624
YR
2625
YI
2626
ZR
2627
ZI
A
B
C
D
AWR
AXR
AYR
AZR
AWI
AXI
AYI
AZI
BWR
BXR
BYR
BZR
BWI
BXI
BYI
BZI
CWR
CXR
CYR
CZR
CWI
CXI
CYI
CZI
DWR
DXR
DYR
DZR
DWI
DXI
DYI
DZI
2633

FIG. 91

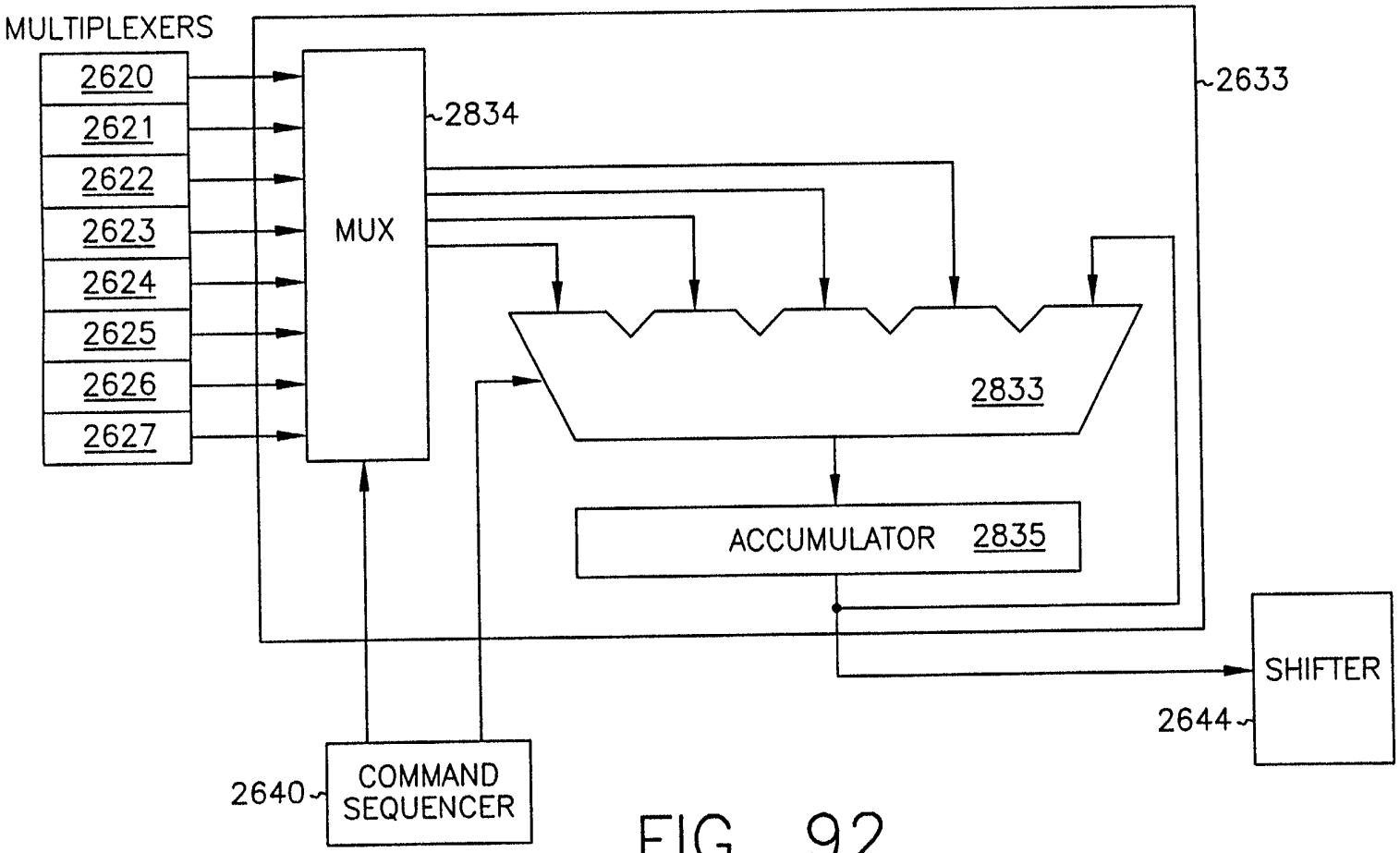

MULTIPLEXERS
2620
2621
2622
2623
2624
2625
2626
2627
MUX
2834
2633
2833
ACCUMULATOR 2835
SHIFTER
2644
2640
COMMAND SEQUENCER

FIG. 92

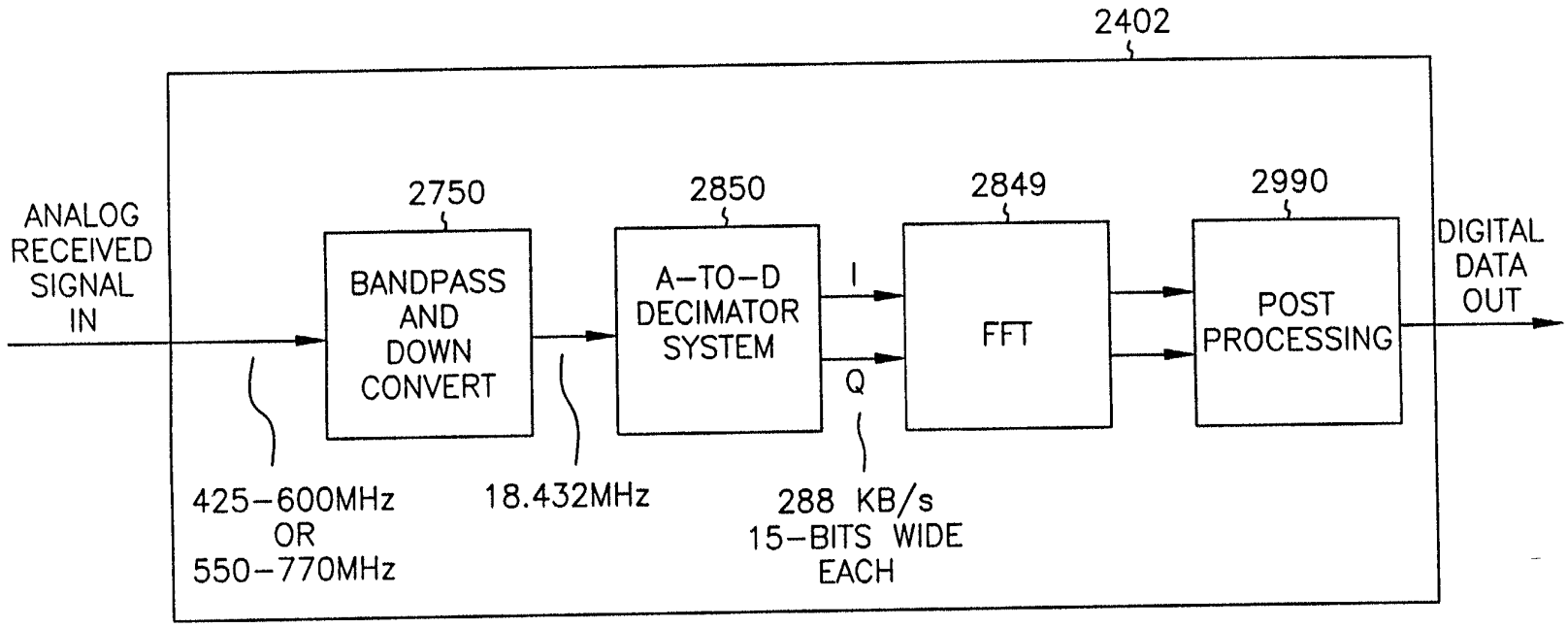

2402
ANALOG RECEIVED SIGNAL IN
2750
BANDPASS AND DOWN CONVERT
2850
A-TO-D DECIMATOR SYSTEM
I
Q
2849
FFT
2990
POST PROCESSING
DIGITAL DATA OUT
425-600MHz OR 550-770MHz
18.432MHz
288 KB/s 15-BITS WIDE EACH

FIG. 93

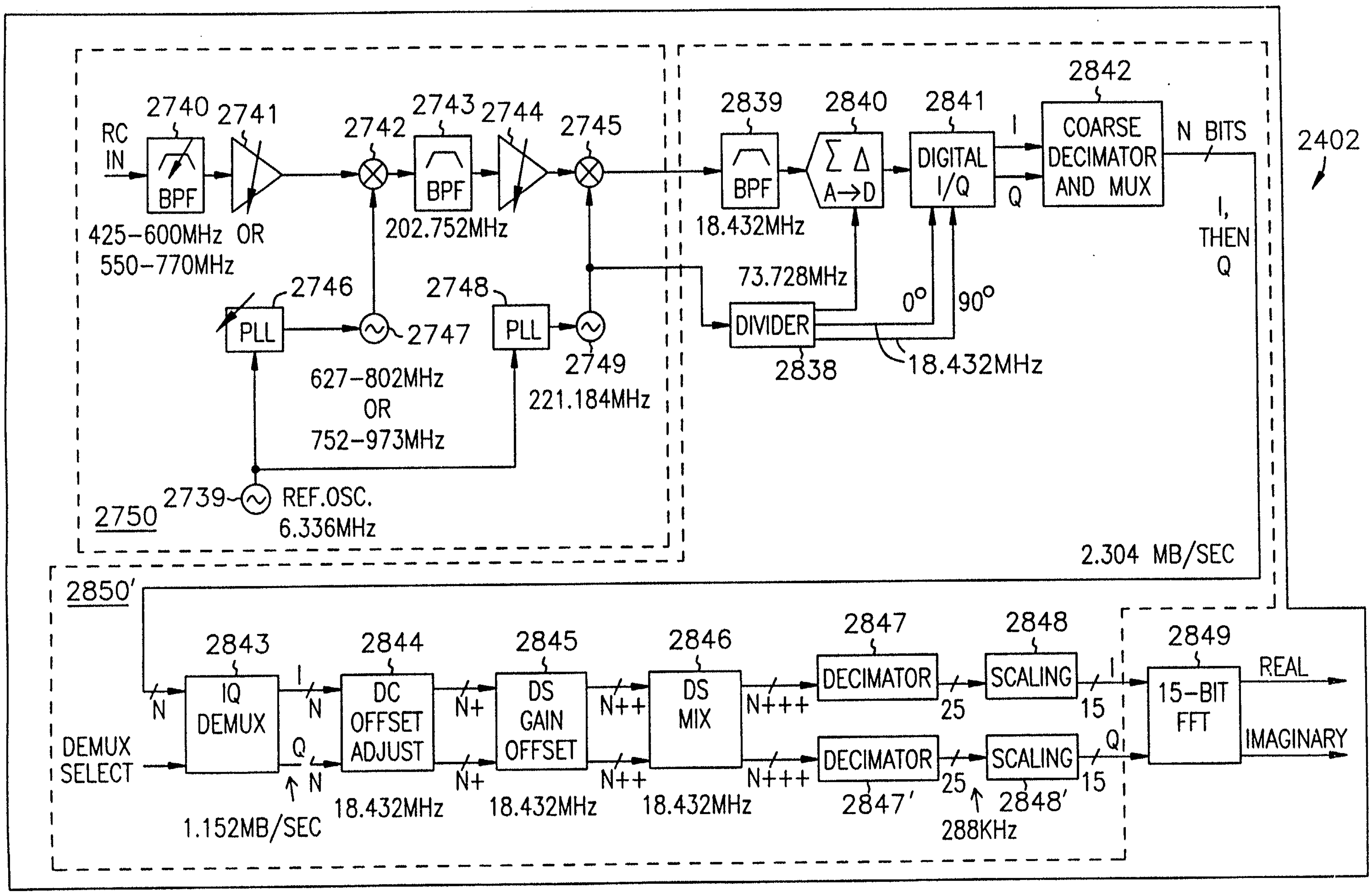

2402
RC IN
2740
BPF
2741
425–600MHz OR
550–770MHz
2742
2743
BPF
2744
202.752MHz
2745
2746
PLL
2747
627–802MHz
OR
752–973MHz
2748
PLL
2749
221.184MHz
2739
REF.OSC.
6.336MHz
2750
2839
BPF
18.432MHz
2840
Σ Δ
A→D
73.728MHz
2838
DIVIDER
2841
DIGITAL I/Q
0°
90°
18.432MHz
I
Q
2842
COARSE DECIMATOR AND MUX
N BITS
I, THEN Q
2.304 MB/SEC
2850′
DEMUX SELECT
2843
IQ DEMUX
N
1.152MB/SEC
2844
DC OFFSET ADJUST
18.432MHz
N+
2845
DS GAIN OFFSET
18.432MHz
N++
2846
DS MIX
18.432MHz
N+++
2847
DECIMATOR
2847′
25
288KHz
2848
SCALING
2848′
15
2849
15–BIT FFT
REAL
IMAGINARY

FIG. 94

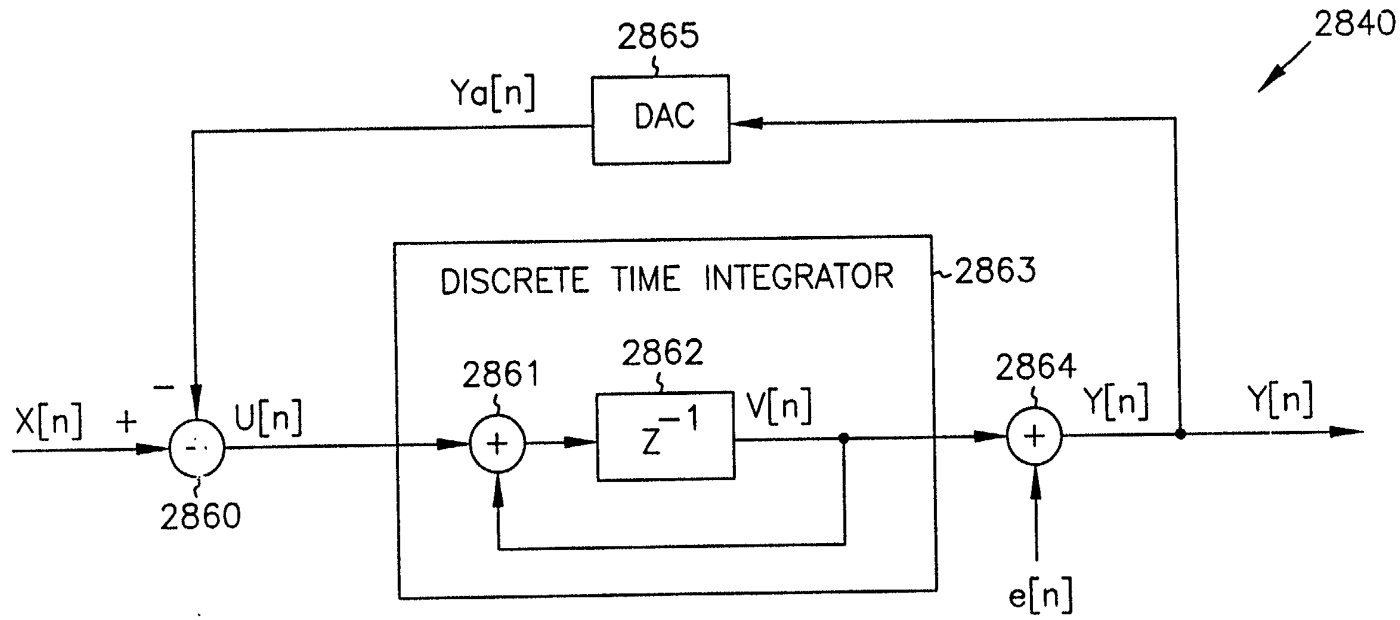


FIG. 95

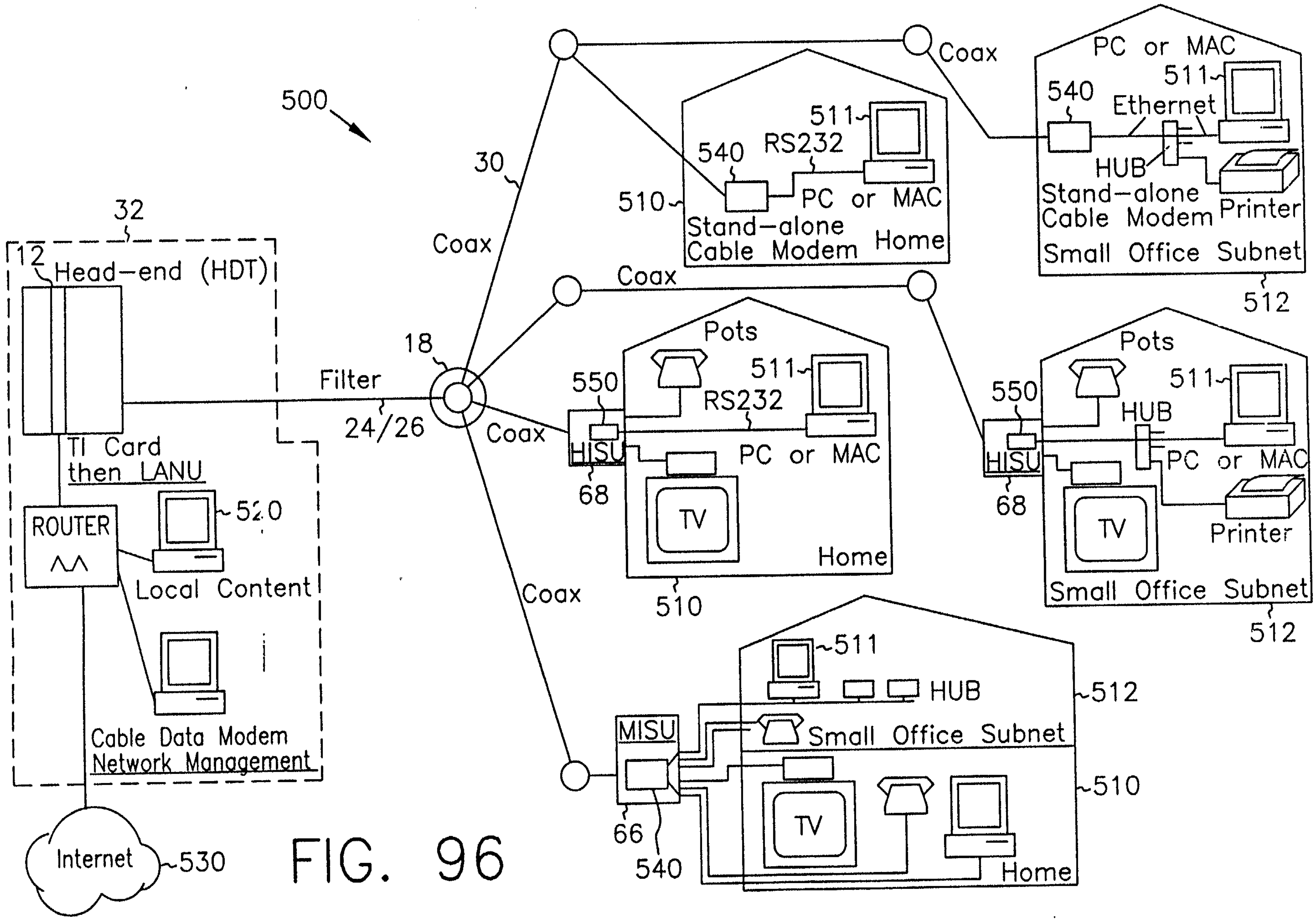

500
32
12
Head-end (HDT)
TI Card
then LANU
ROUTER
520
Local Content
Cable Data Modem
Network Management
Internet
530
Filter
24/26
18
30
Coax
Coax
Coax
Coax
Coax
Coax
510
540
RS232
511
PC or MAC
Stand-alone
Cable Modem
Home
PC or MAC
540
511
Ethernet
HUB
Stand-alone
Cable Modem
Printer
Small Office Subnet
512
550
Pots
511
RS232
HISU
68
PC or MAC
TV
Home
510
550
Pots
511
HUB
HISU
68
PC or MAC
TV
Printer
Small Office Subnet
512
511
HUB
512
MISU
Small Office Subnet
510
66
540
TV
Home

FIG. 96

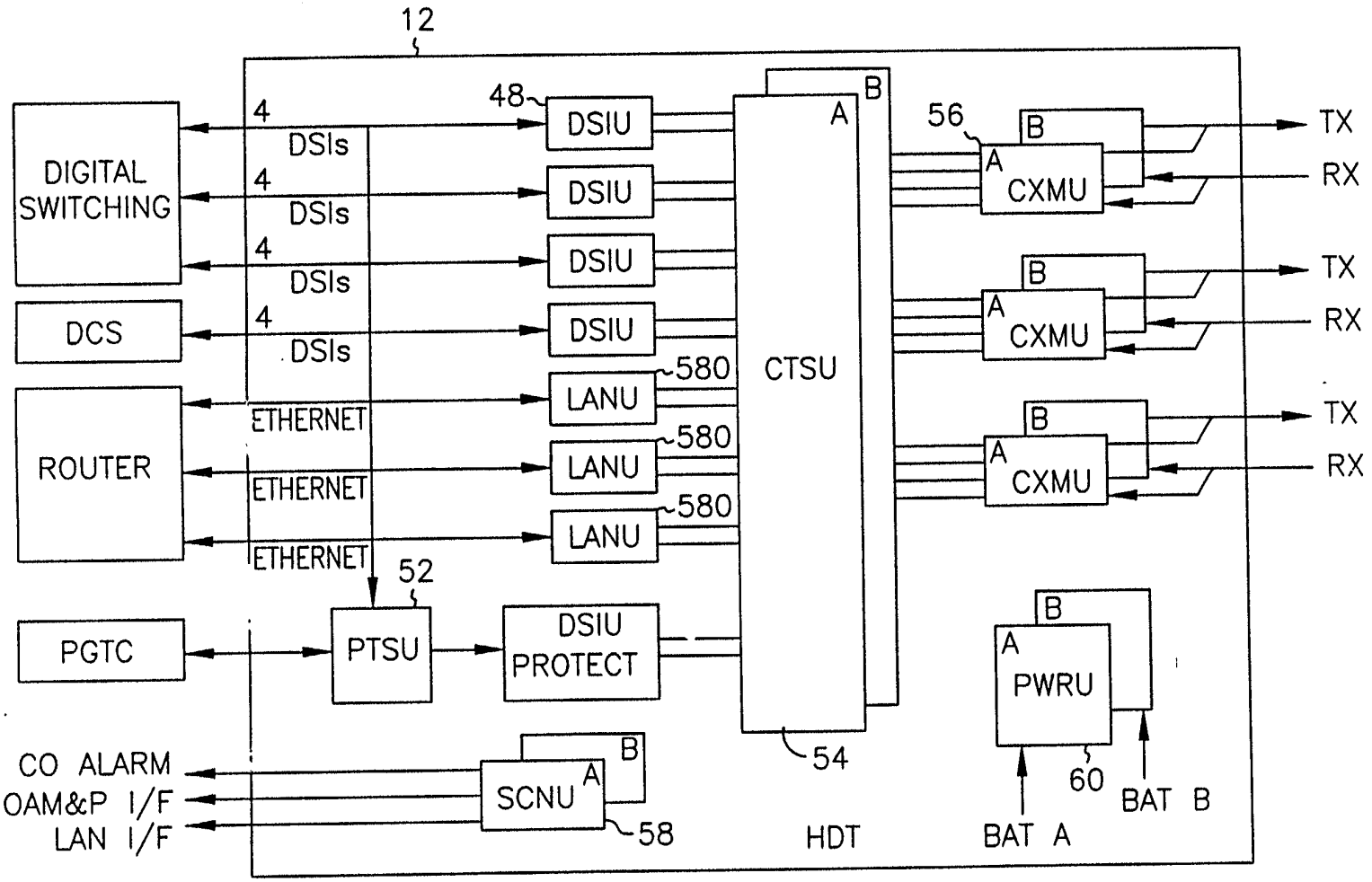

12
DIGITAL SWITCHING
DCS
ROUTER
PGTC
4 DSIs
4 DSIs
4 DSIs
4 DSIs
ETHERNET
ETHERNET
ETHERNET
48
DSIU
DSIU
DSIU
DSIU
LANU
LANU
LANU
580
580
580
52
PTSU
DSIU PROTECT
CTSU
A
B
54
HDT
56
CXMU
CXMU
CXMU
TX
RX
TX
RX
TX
RX
PWRU
60
BAT A
BAT B
CO ALARM
OAM&P I/F
LAN I/F
SCNU
58

FIG. 97

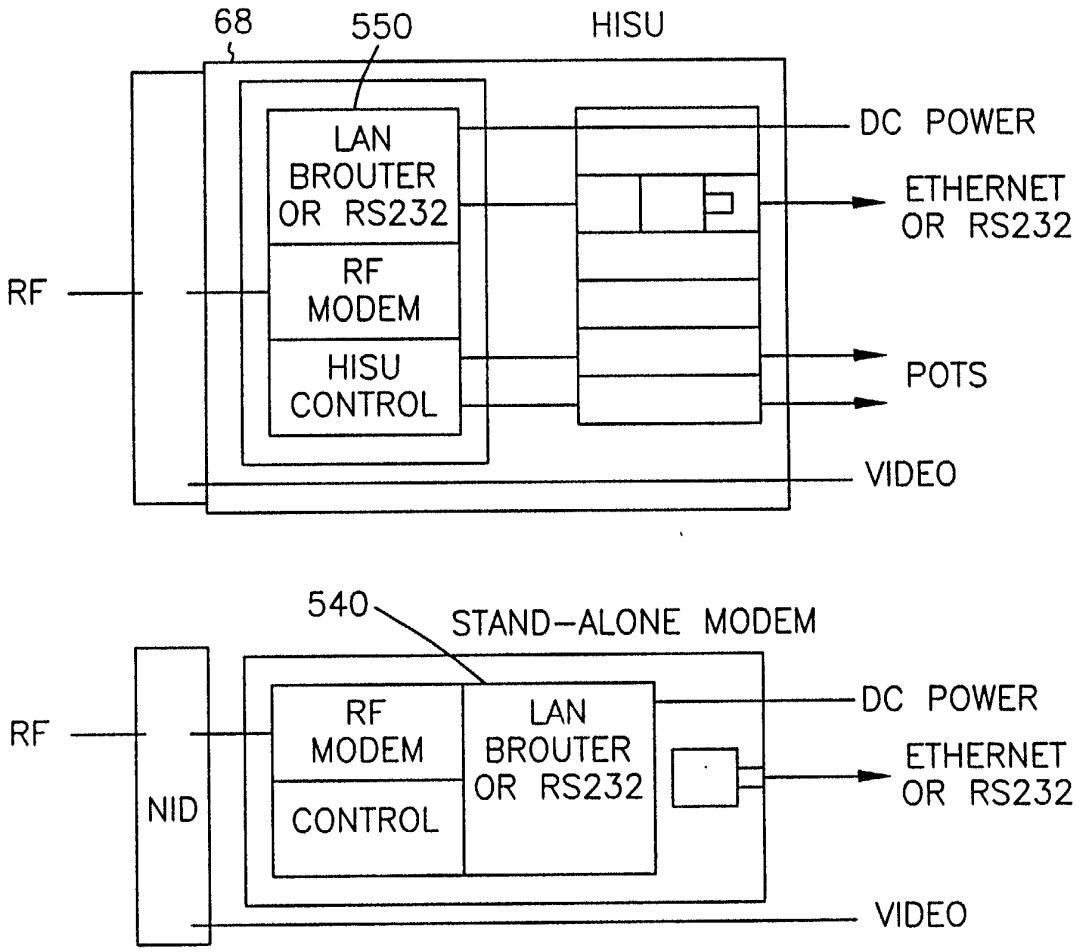

68
550
HISU
LAN
BROUTER
OR RS232
RF
MODEM
HISU
CONTROL
RF
DC POWER
ETHERNET
OR RS232
POTS
VIDEO
540
STAND-ALONE MODEM
RF
NID
RF
MODEM
CONTROL
LAN
BROUTER
OR RS232
DC POWER
ETHERNET
OR RS232
VIDEO

FIG. 98

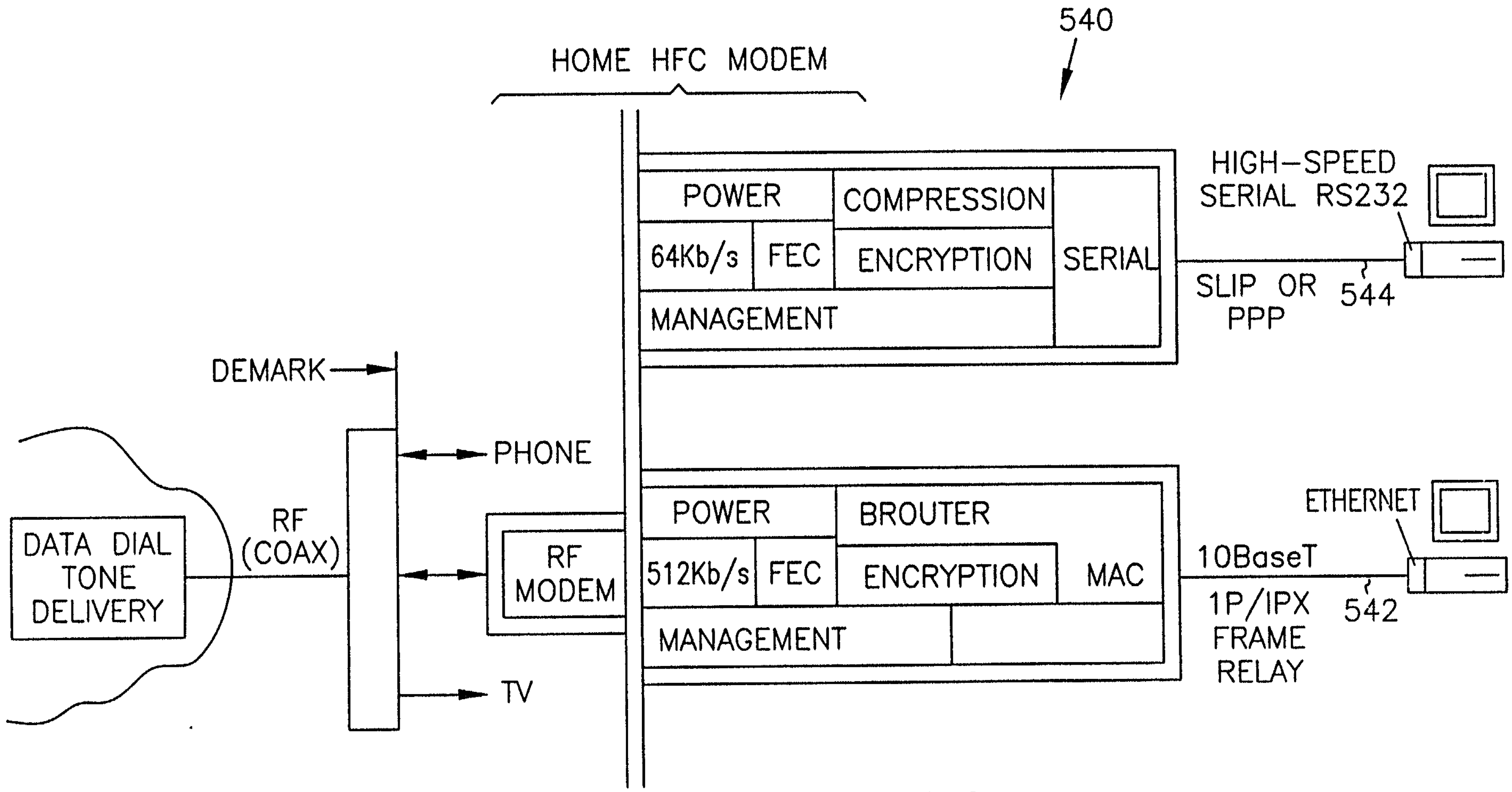


FIG. 99

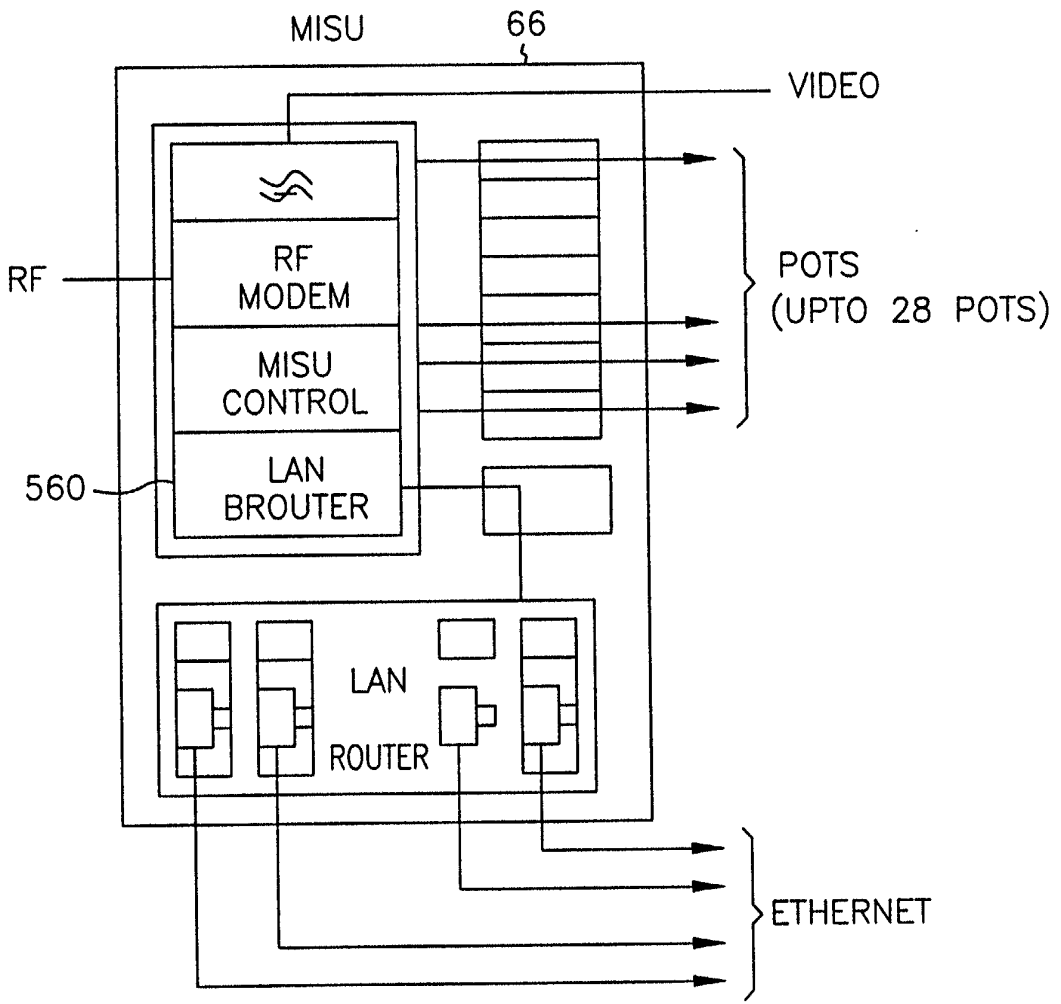
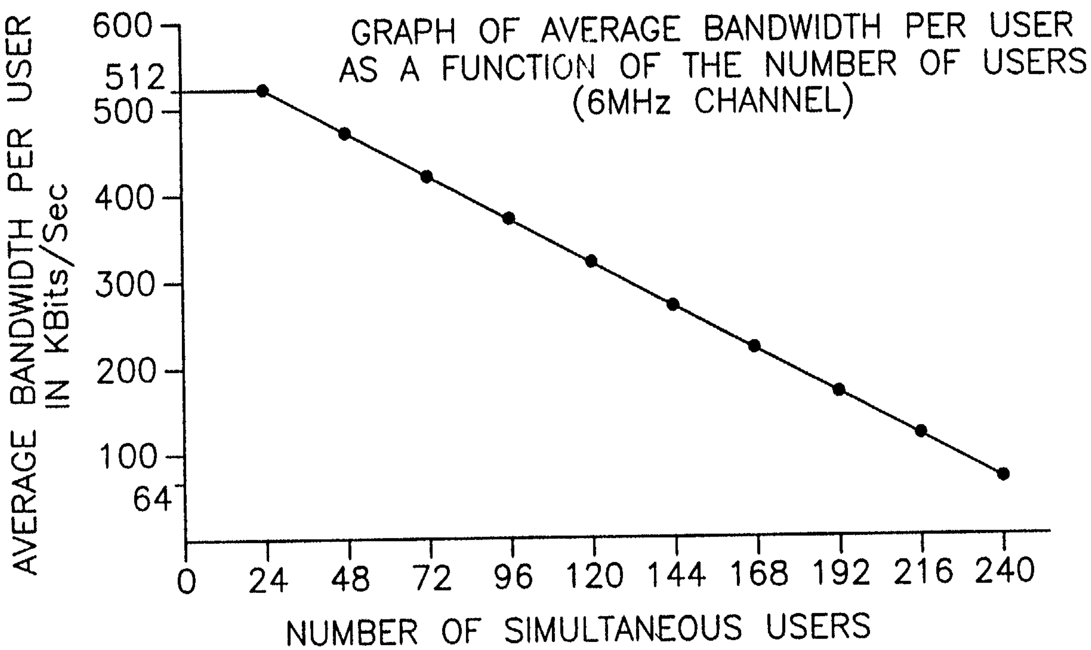

MISU
66
VIDEO
RF
RF MODEM
MISU CONTROL
LAN BROUTER
560
POTS
(UPTO 28 POTS)
LAN
ROUTER
ETHERNET

FIG. 100



GRAPH OF AVERAGE BANDWIDTH PER USER
AS A FUNCTION OF THE NUMBER OF USERS
(6MHz CHANNEL)
AVERAGE BANDWIDTH PER USER
IN KBits/Sec
600
512
500
400
300
200
100
64
0
24
48
72
96
120
144
168
192
216
240
NUMBER OF SIMULTANEOUS USERS

FIG. 101

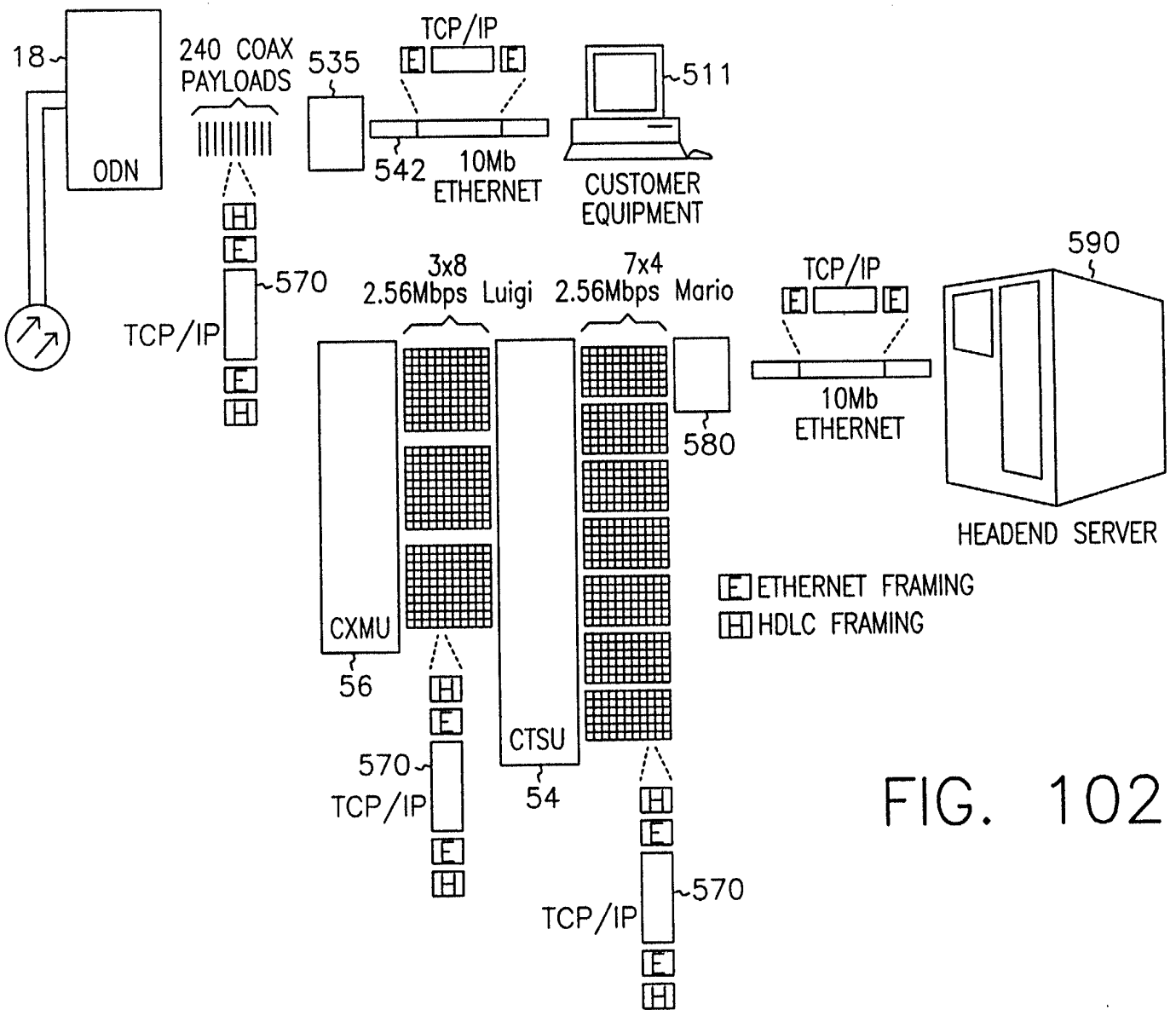

18
ODN
240 COAX PAYLOADS
535
TCP/IP
542
10Mb ETHERNET
511
CUSTOMER EQUIPMENT
590
HEADEND SERVER
570
TCP/IP
3x8 2.56Mbps Luigi
7x4 2.56Mbps Mario
580
CXMU
56
CTSU
54
E ETHERNET FRAMING
H HDLC FRAMING

FIG. 102

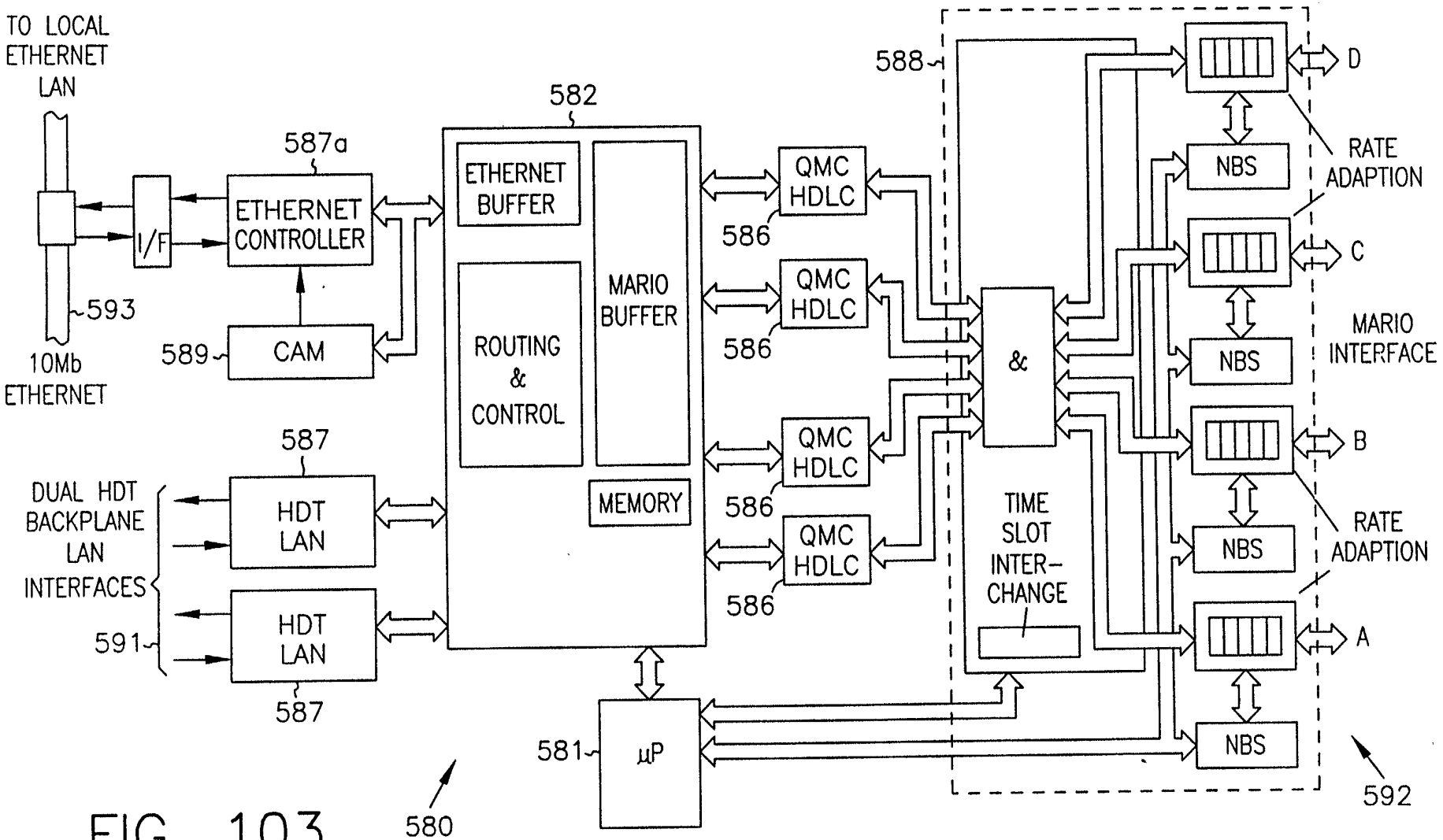

TO LOCAL ETHERNET LAN
10Mb ETHERNET
593
I/F
587a
ETHERNET CONTROLLER
589
CAM
582
ETHERNET BUFFER
ROUTING & CONTROL
MARIO BUFFER
MEMORY
587
DUAL HDT BACKPLANE LAN INTERFACES
591
HDT LAN
HDT LAN
587
581
µP
580
QMC HDLC
QMC HDLC
QMC HDLC
QMC HDLC
586
586
586
586
588
&
TIME SLOT INTER-CHANGE
NBS
NBS
NBS
NBS
RATE ADAPTION
RATE ADAPTION
MARIO INTERFACE
D
C
B
A
592

FIG. 103

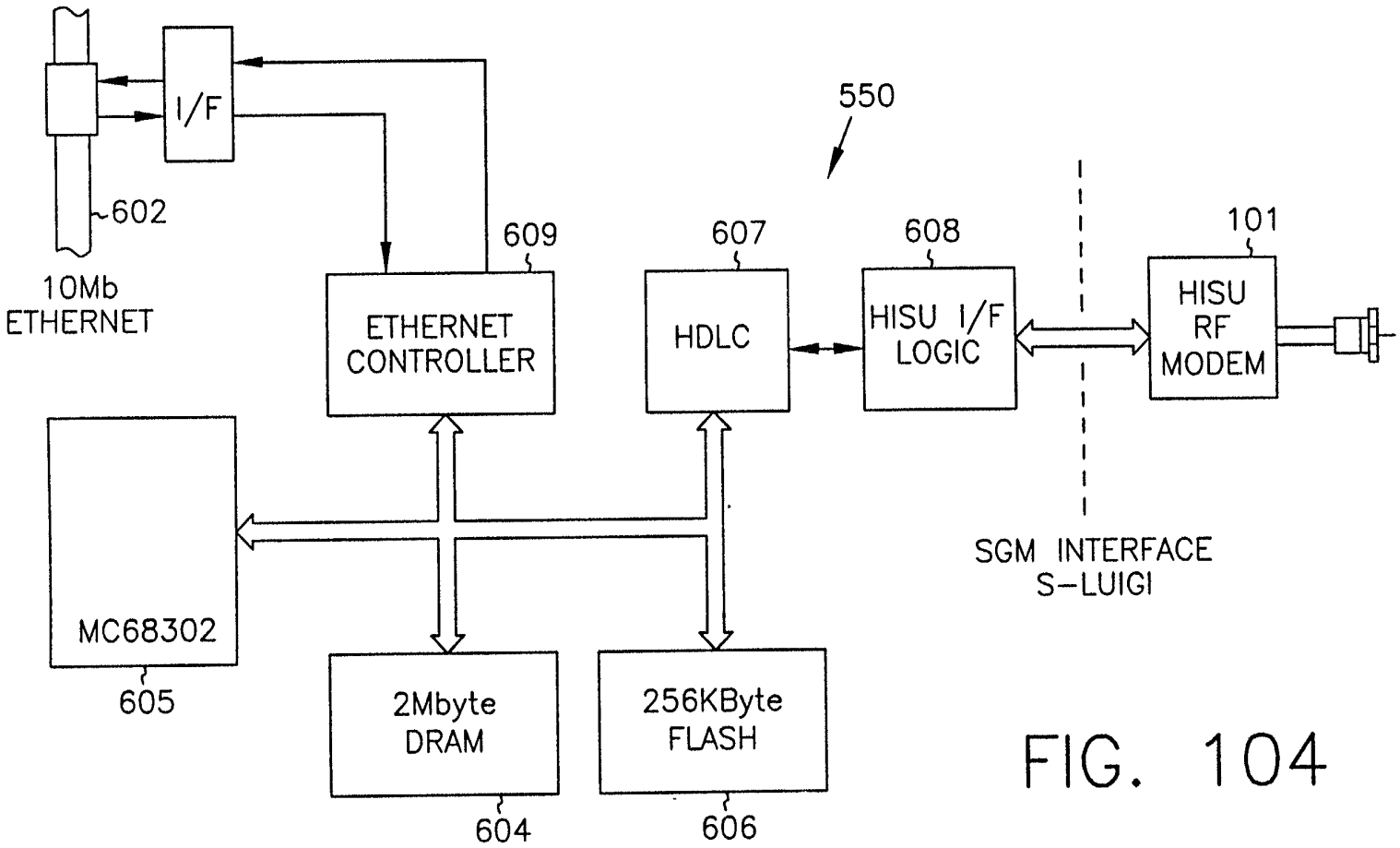

I/F
602
10Mb
ETHERNET
609
ETHERNET
CONTROLLER
550
607
HDLC
608
HISU I/F
LOGIC
101
HISU
RF
MODEM
SGM INTERFACE
S-LUIGI
MC68302
605
2Mbyte
DRAM
604
256KByte
FLASH
606

FIG. 104

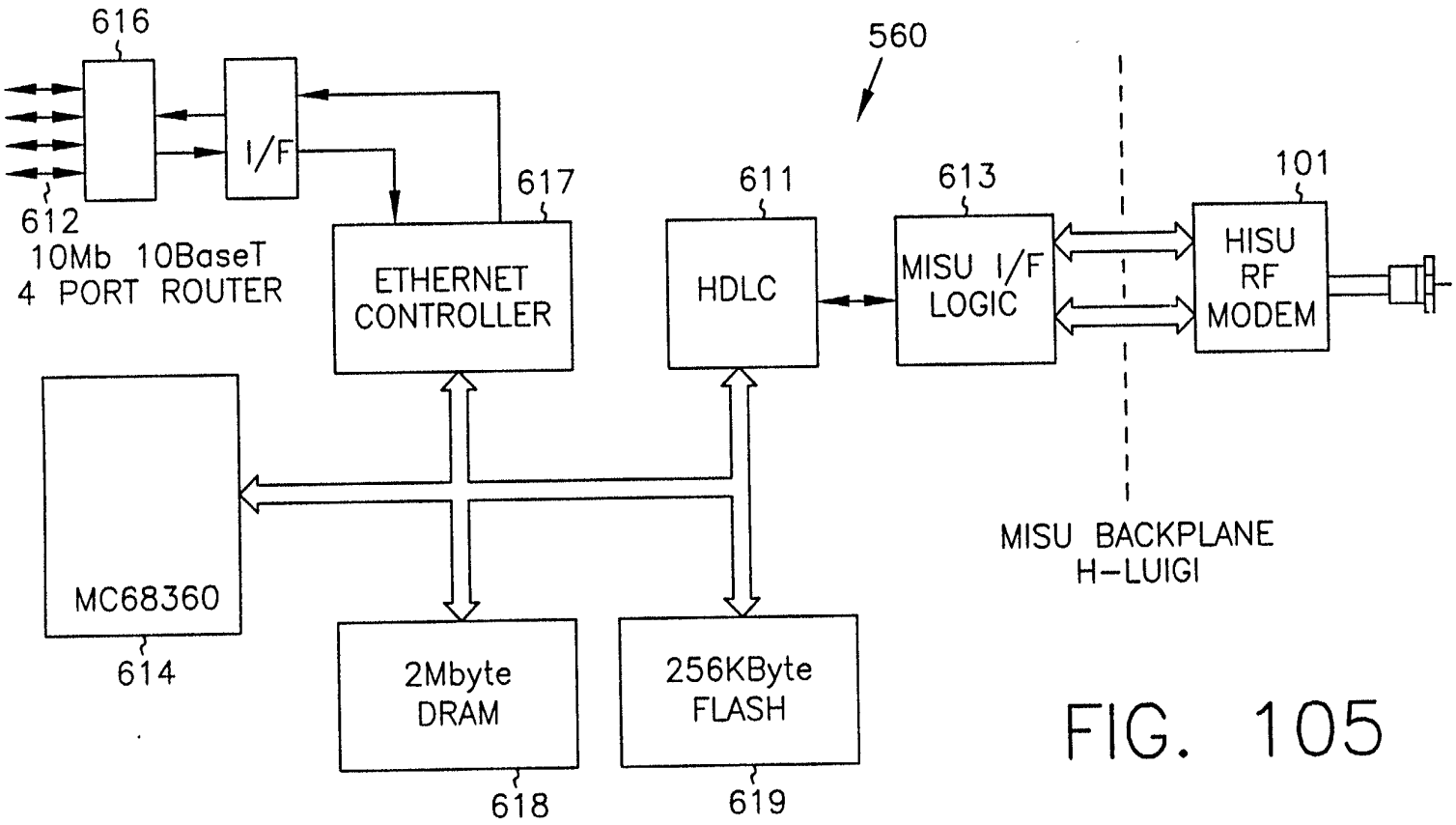

616
560
I/F
617
611
613
101
612
10Mb 10BaseT
4 PORT ROUTER
ETHERNET
CONTROLLER
HDLC
MISU I/F
LOGIC
HISU
RF
MODEM
MISU BACKPLANE
H-LUIGI
MC68360
614
2Mbyte
DRAM
618
256KByte
FLASH
619

FIG. 105

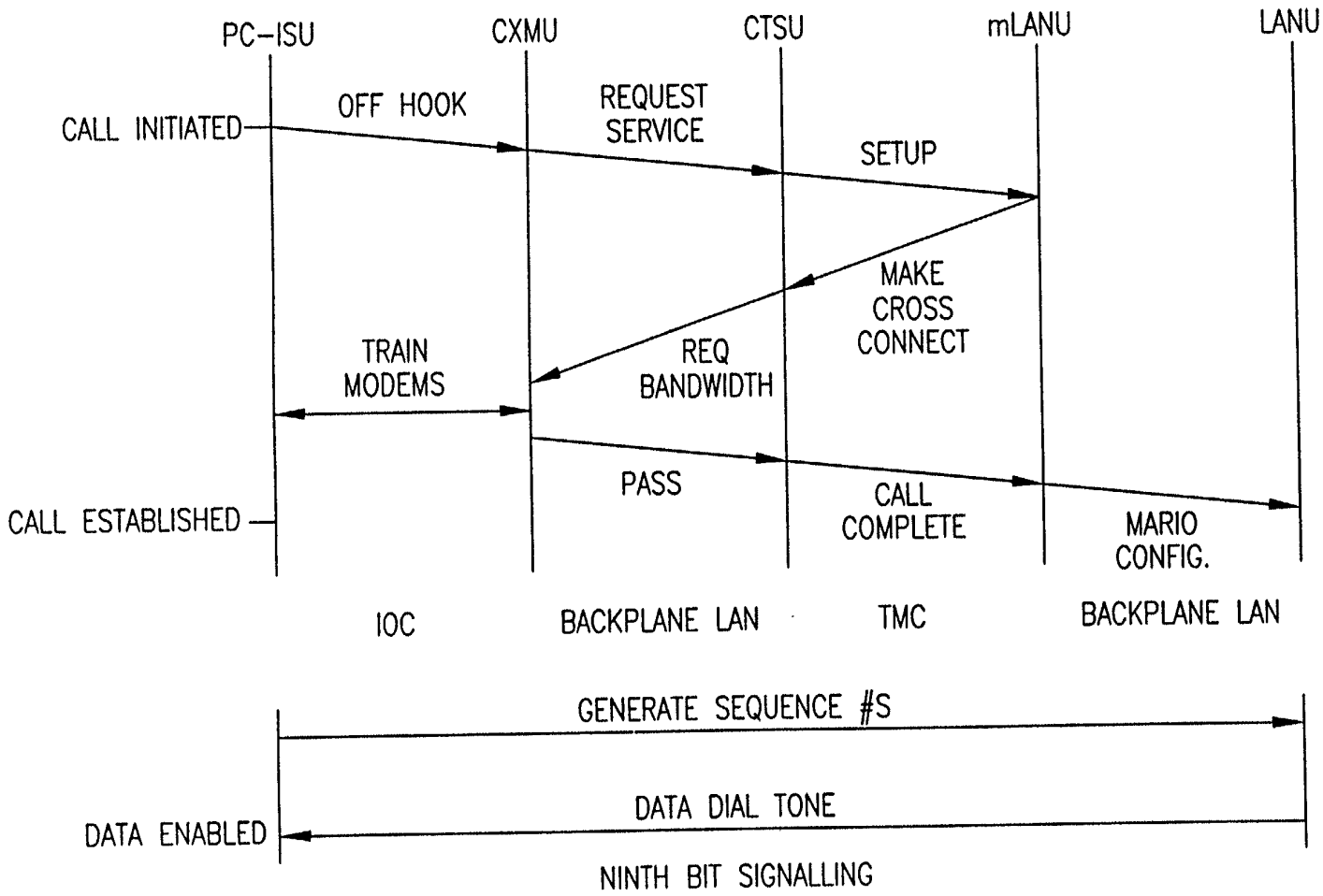

PC-ISU
CXMU
CTSU
mLANU
LANU
CALL INITIATED
OFF HOOK
REQUEST SERVICE
SETUP
MAKE CROSS CONNECT
TRAIN MODEMS
REQ BANDWIDTH
PASS
CALL ESTABLISHED
CALL COMPLETE
MARIO CONFIG.
IOC
BACKPLANE LAN
TMC
BACKPLANE LAN
GENERATE SEQUENCE #S
DATA DIAL TONE
DATA ENABLED
NINTH BIT SIGNALLING

FIG. 106

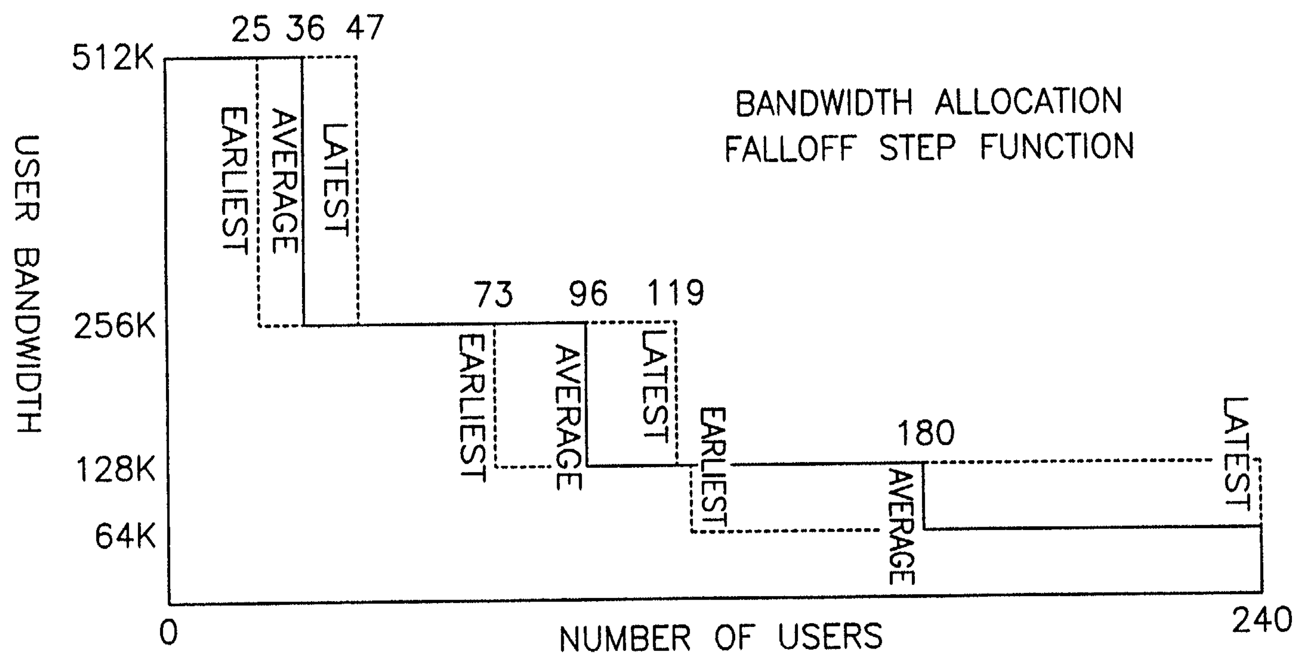
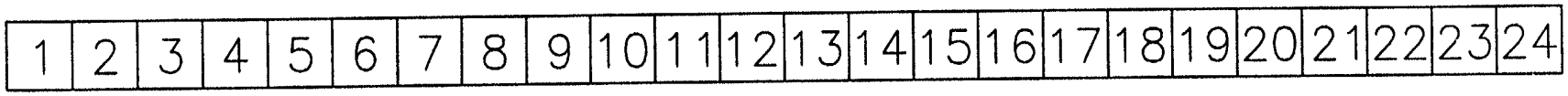
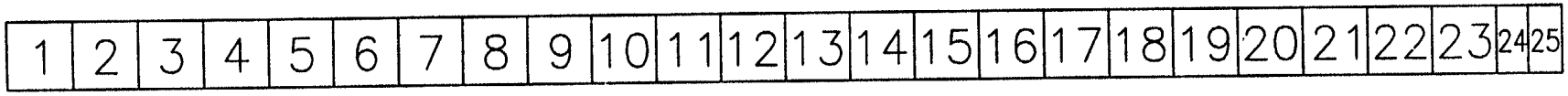

BANDWIDTH ALLOCATION
FALLOFF STEP FUNCTION
USER BANDWIDTH
512K
256K
128K
64K
0
NUMBER OF USERS
240
25 36 47
EARLIEST
AVERAGE
LATEST
73
96
119
EARLIEST
AVERAGE
LATEST
180
EARLIEST
AVERAGE
LATEST

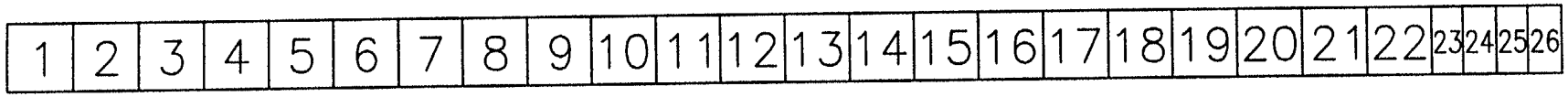
FIG. 107



THE RF SPECTRUM OF 24 USERS WITH 512Kbs



ADDING THE 25th USER



ADDING THE 26th USER, ETC

FIG. 108

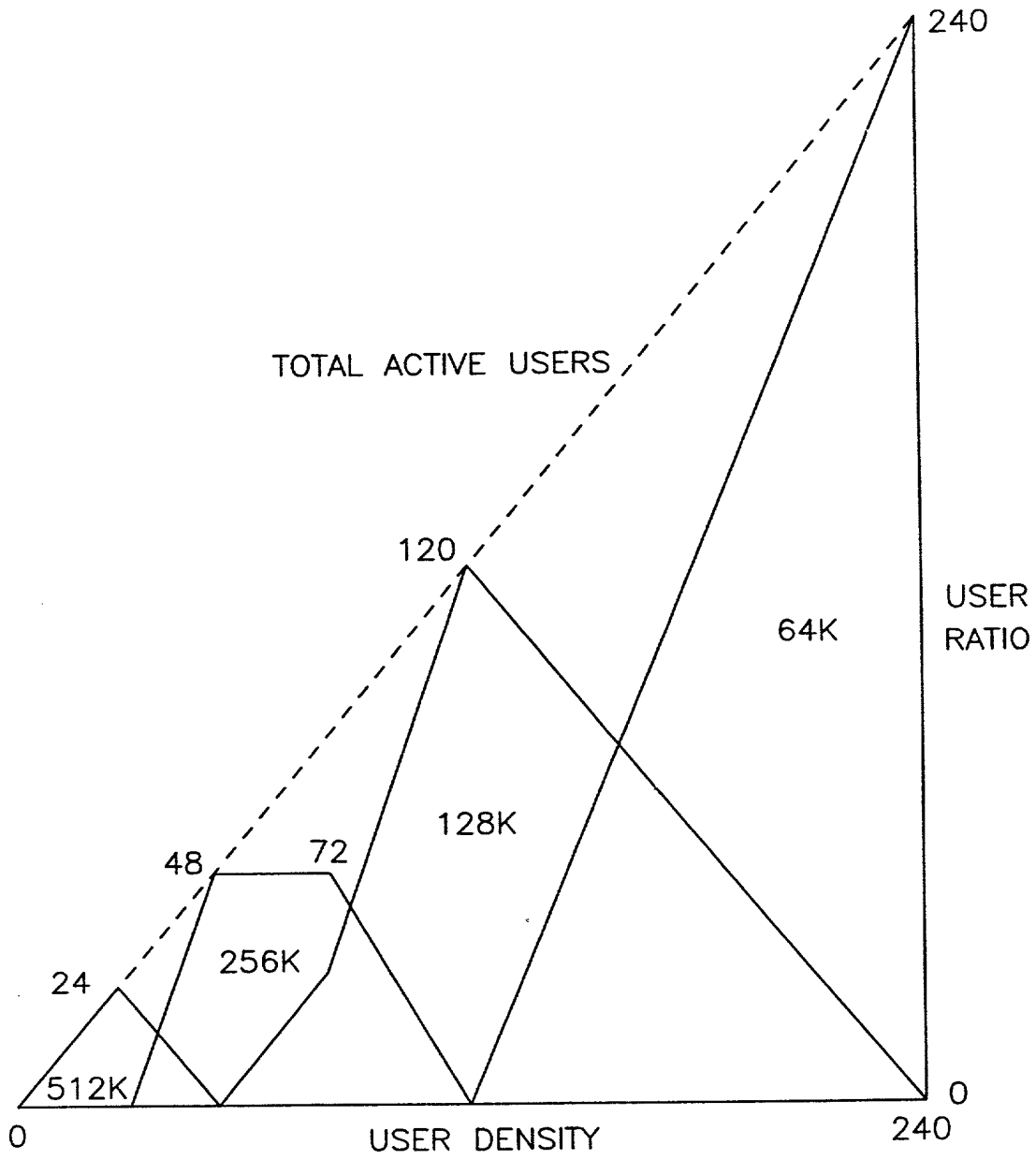

240
TOTAL ACTIVE USERS
120
USER
RATIO
64K
128K
48
72
256K
24
512K
0
0
USER DENSITY
240

FIG. 109

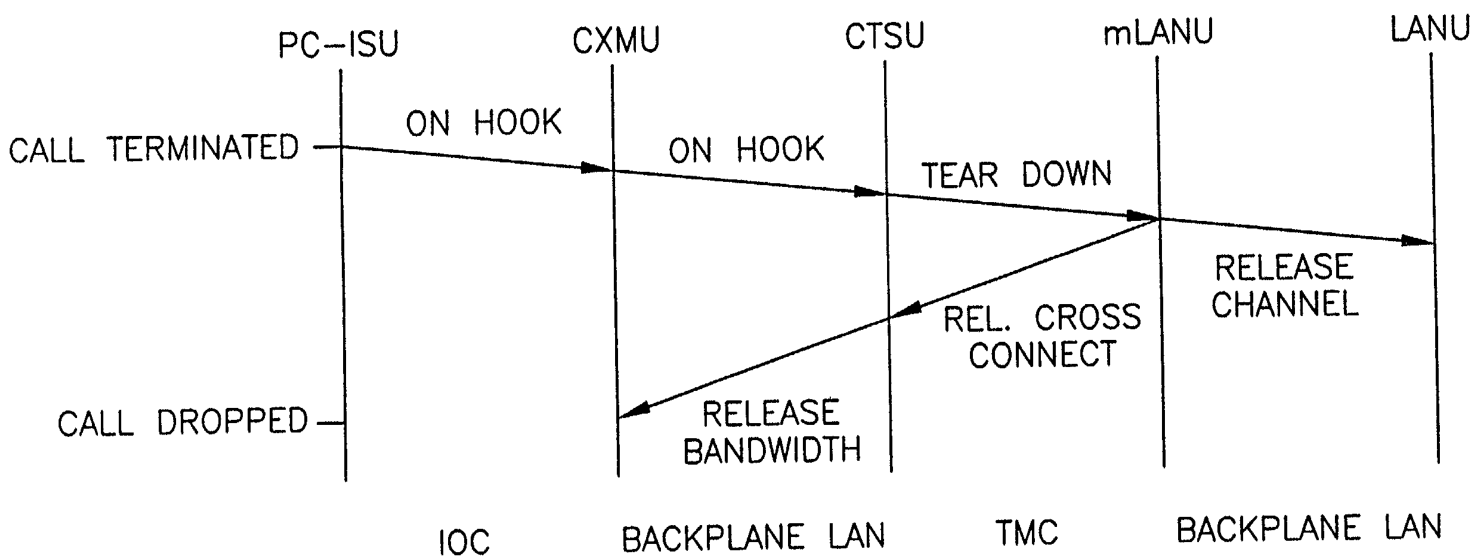

PC–ISU
CXMU
CTSU
mLANU
LANU
CALL TERMINATED
ON HOOK
ON HOOK
TEAR DOWN
RELEASE CHANNEL
REL. CROSS CONNECT
RELEASE BANDWIDTH
CALL DROPPED
IOC
BACKPLANE LAN
TMC
BACKPLANE LAN

FIG. 110

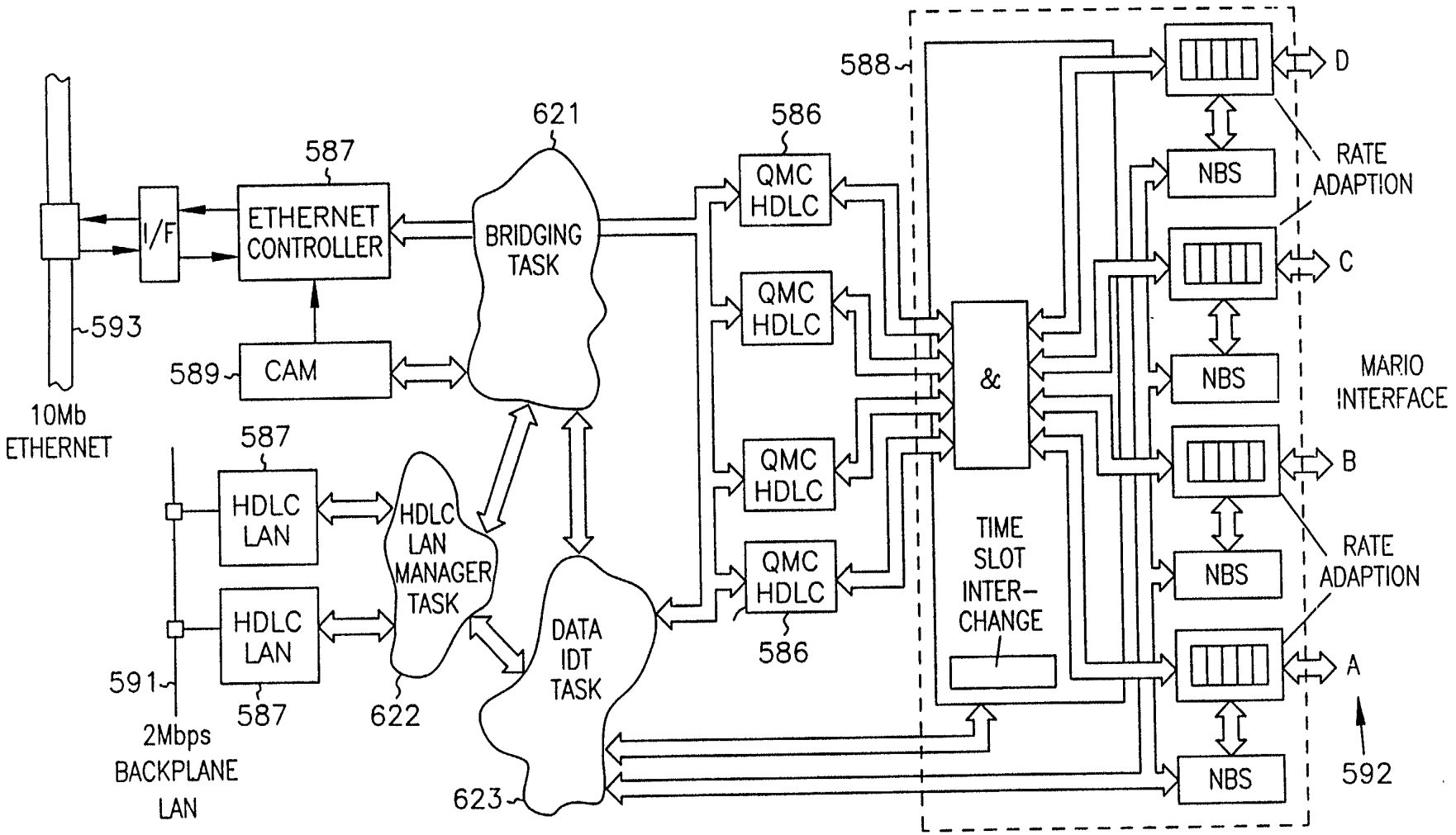

588
621
586
587
QMC HDLC
NBS
RATE ADAPTION
D
I/F
ETHERNET CONTROLLER
BRIDGING TASK
C
593
589
CAM
&
MARIO INTERFACE
10Mb ETHERNET
587
HDLC LAN
HDLC LAN MANAGER TASK
B
TIME SLOT INTER-CHANGE
RATE ADAPTION
HDLC LAN
DATA IDT TASK
A
591
587
622
586
2Mbps BACKPLANE LAN
623
592
620

FIG. 111

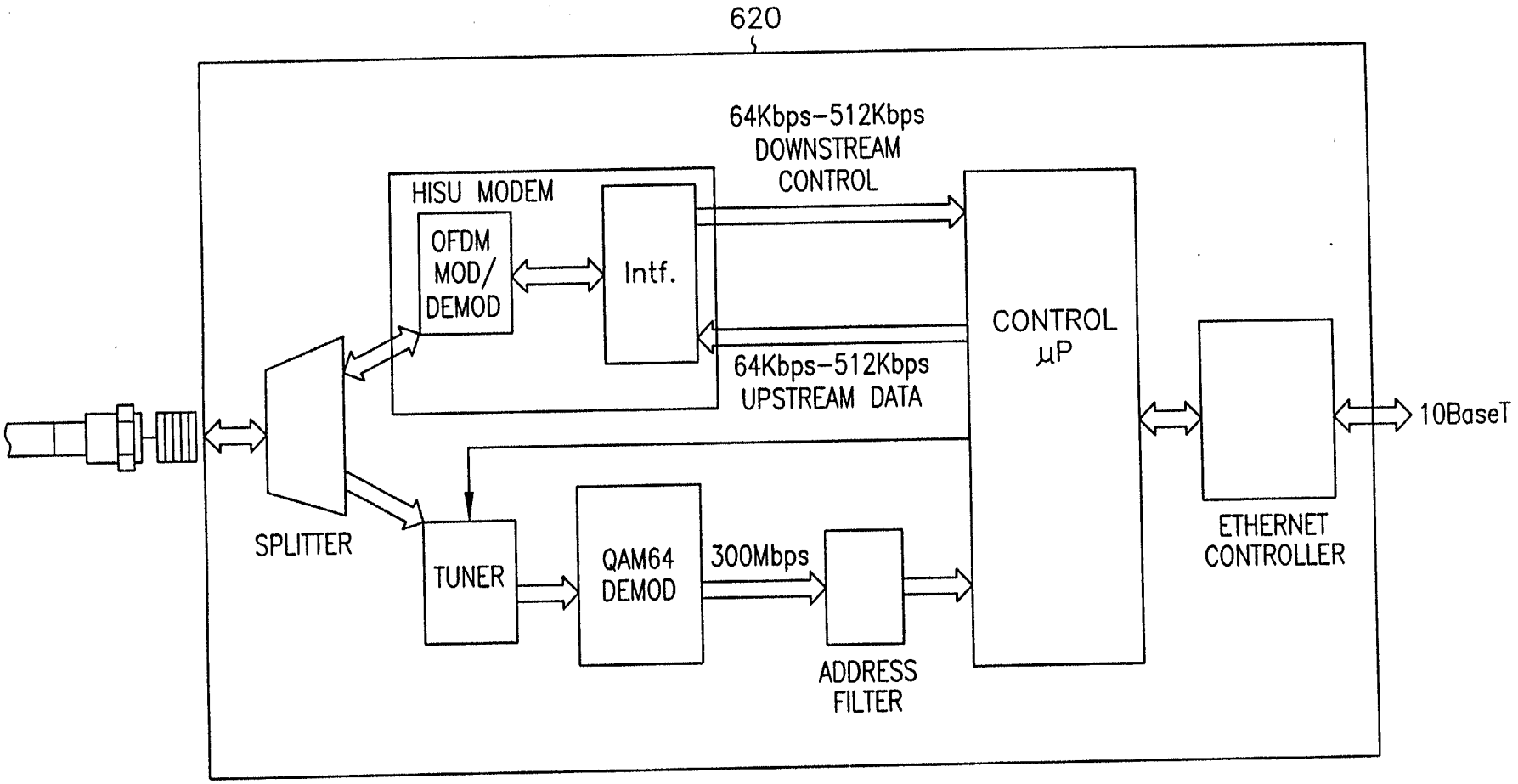

620
64Kbps-512Kbps
DOWNSTREAM
CONTROL
HISU MODEM
OFDM
MOD/
DEMOD
Intf.
CONTROL
μP
64Kbps-512Kbps
UPSTREAM DATA
10BaseT
SPLITTER
TUNER
QAM64
DEMOD
300Mbps
ETHERNET
CONTROLLER
ADDRESS
FILTER

FIG. 112

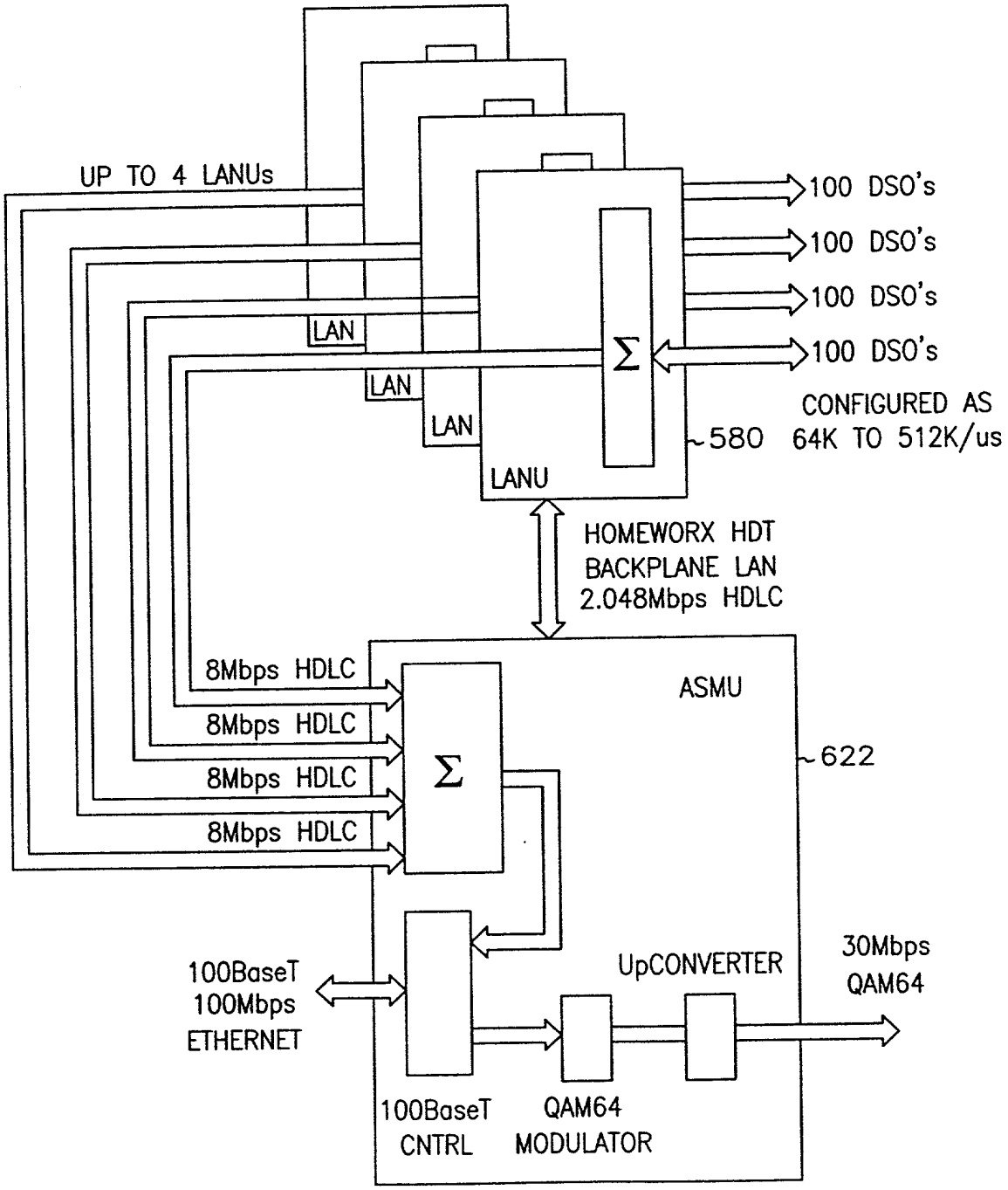

UP TO 4 LANUs
100 DSO's
100 DSO's
100 DSO's
100 DSO's
LAN
LAN
LAN
LANU
Σ
CONFIGURED AS
64K TO 512K/us
~580
HOMEWORX HDT
BACKPLANE LAN
2.048Mbps HDLC
8Mbps HDLC
8Mbps HDLC
8Mbps HDLC
8Mbps HDLC
ASMU
~622
Σ
100BaseT
100Mbps
ETHERNET
UpCONVERTER
30Mbps
QAM64
100BaseT
CNTRL
QAM64
MODULATOR

FIG. 113

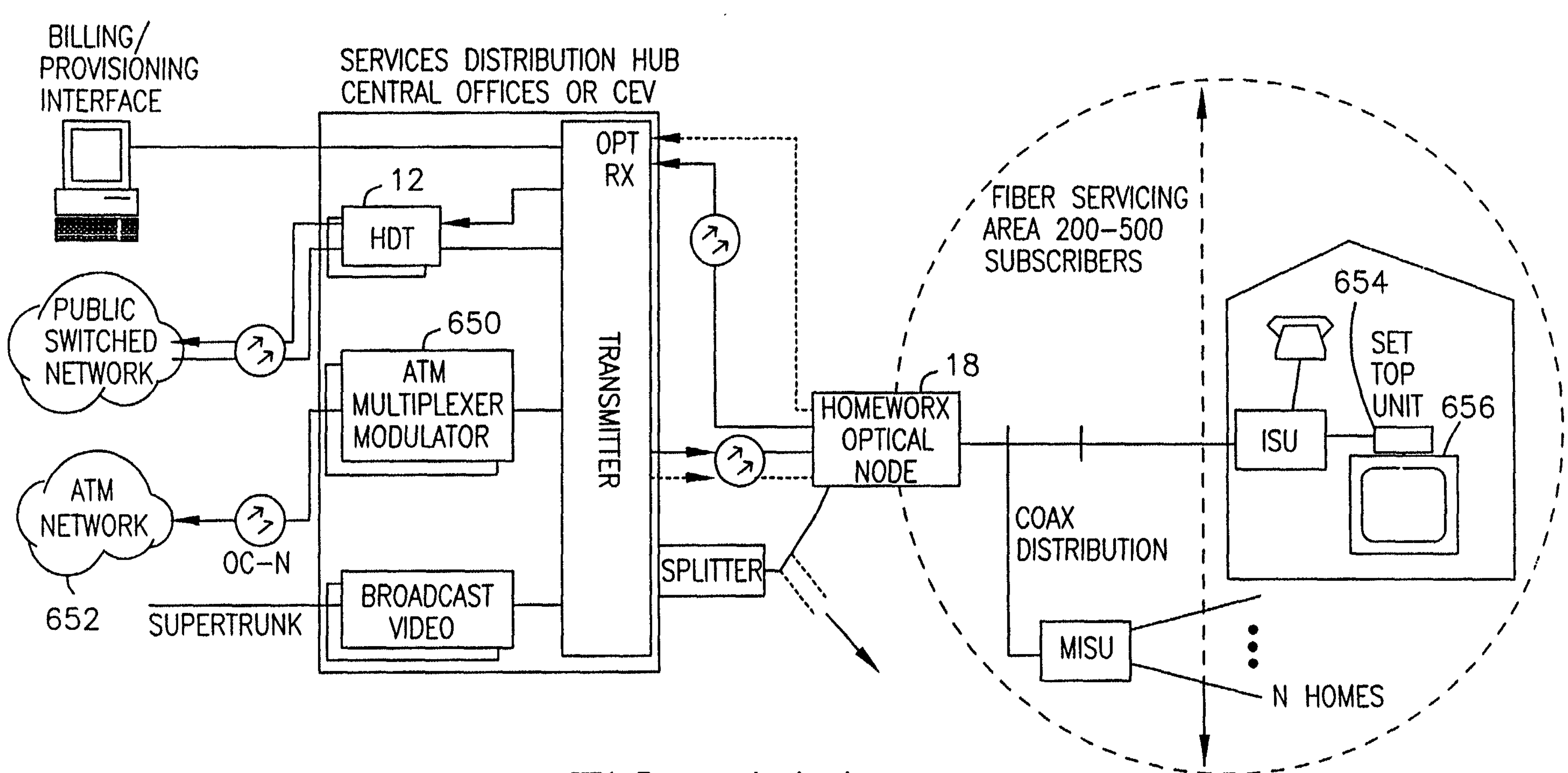

BILLING/
PROVISIONING
INTERFACE
SERVICES DISTRIBUTION HUB
CENTRAL OFFICES OR CEV
OPT
RX
12
HDT
PUBLIC
SWITCHED
NETWORK
650
ATM
MULTIPLEXER
MODULATOR
TRANSMITTER
ATM
NETWORK
OC–N
652
SUPERTRUNK
BROADCAST
VIDEO
SPLITTER
18
HOMEWORX
OPTICAL
NODE
FIBER SERVICING
AREA 200–500
SUBSCRIBERS
654
SET
TOP
UNIT
656
ISU
COAX
DISTRIBUTION
MISU
N HOMES

FIG. 114

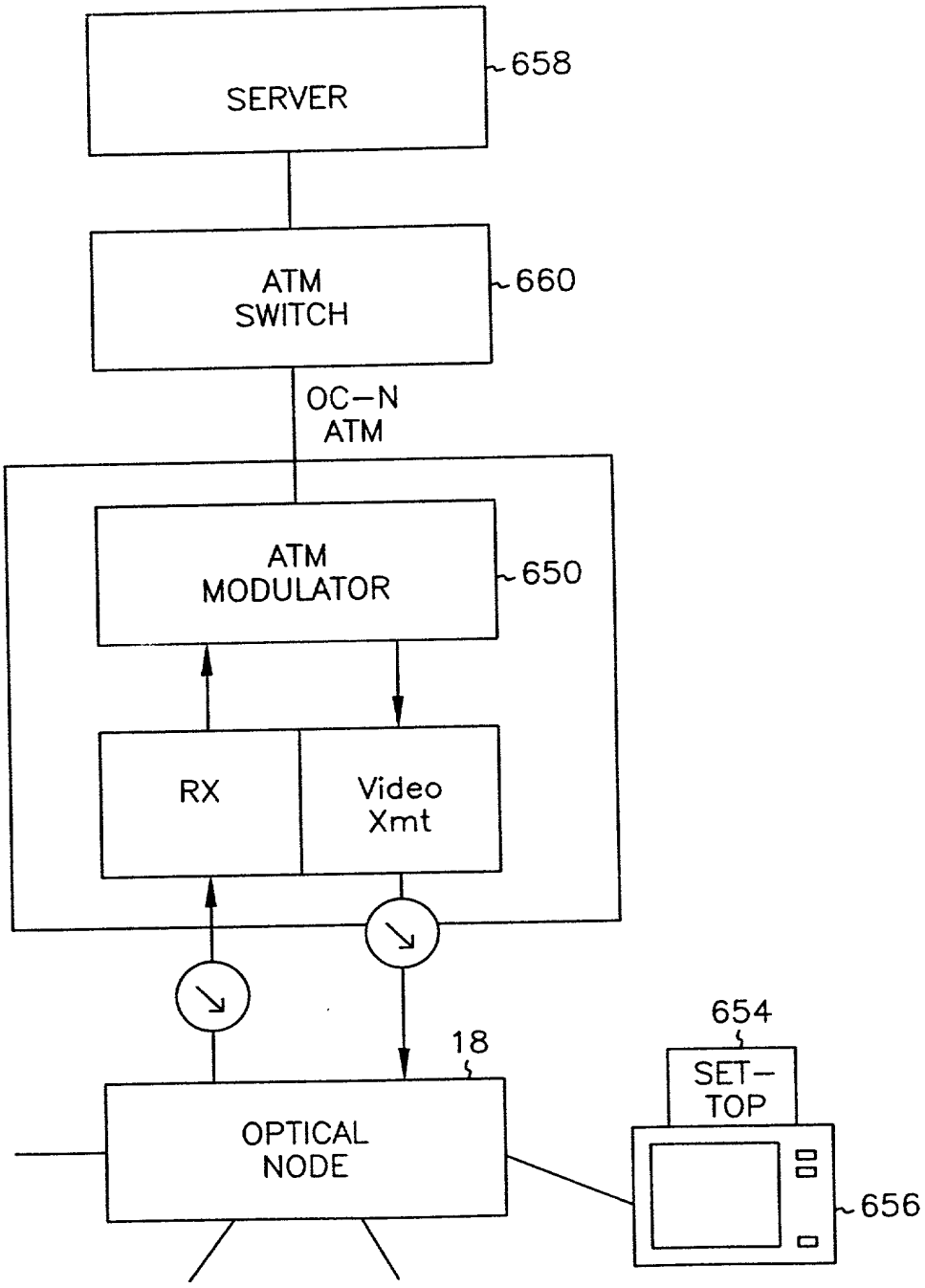

SERVER
658
ATM
SWITCH
660
OC–N
ATM
ATM
MODULATOR
650
RX
Video
Xmt
18
654
SET–
TOP
OPTICAL
NODE
656

FIG. 115

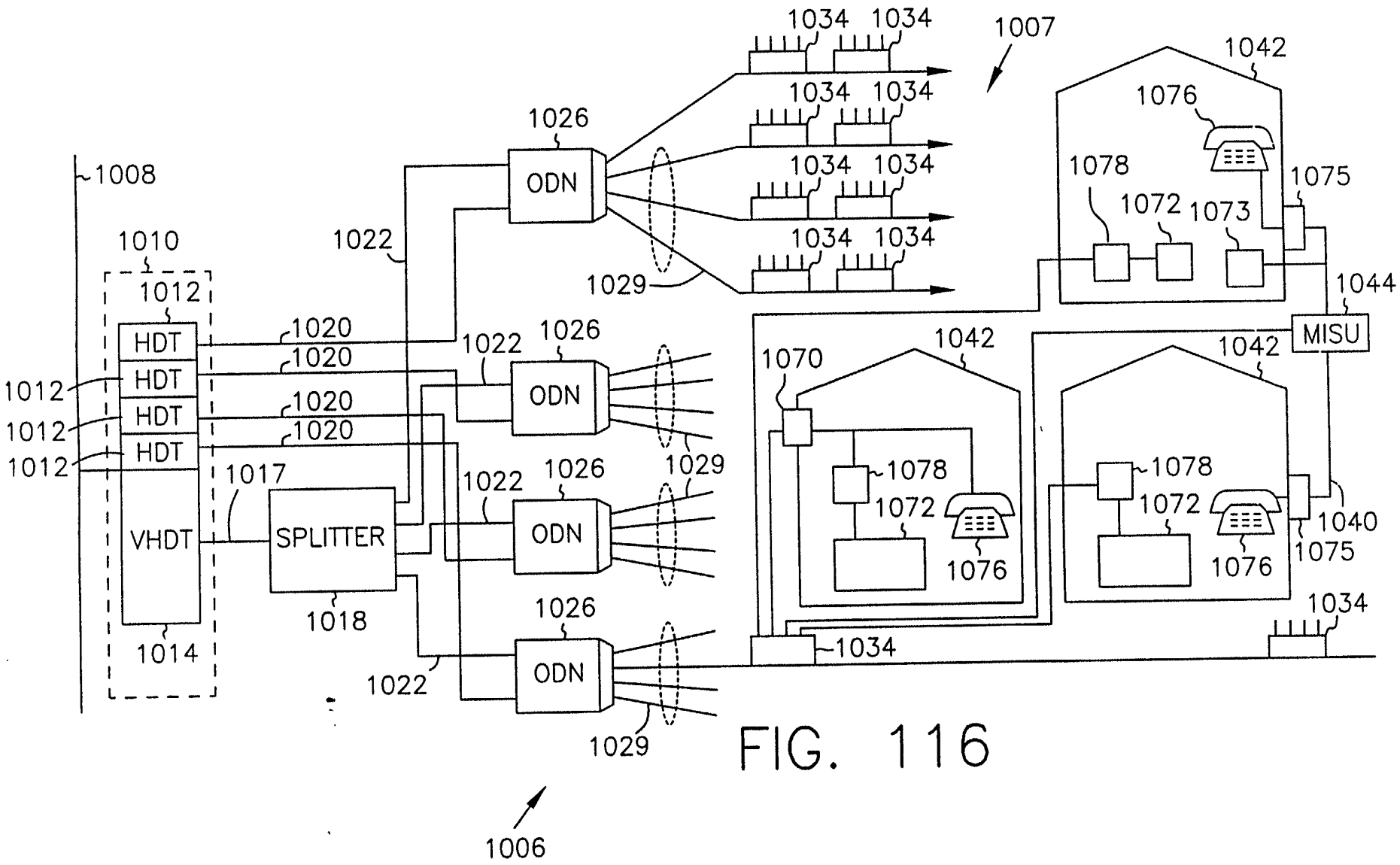

1008
1010
1012
HDT
HDT
HDT
VHDT
1014
1012
1012
1012
1017
SPLITTER
1018
1020
1020
1020
1020
1022
1022
1022
1026
ODN
1026
ODN
1026
ODN
1029
1029
1029
1034 1034
1034 1034
1034 1034
1034 1034
1007
1042
1076
1078
1072
1073
1075
1044
MISU
1042
1070
1078
1072
1076
1042
1078
1072
1076
1040
1075
1034
1034
1006

FIG. 116

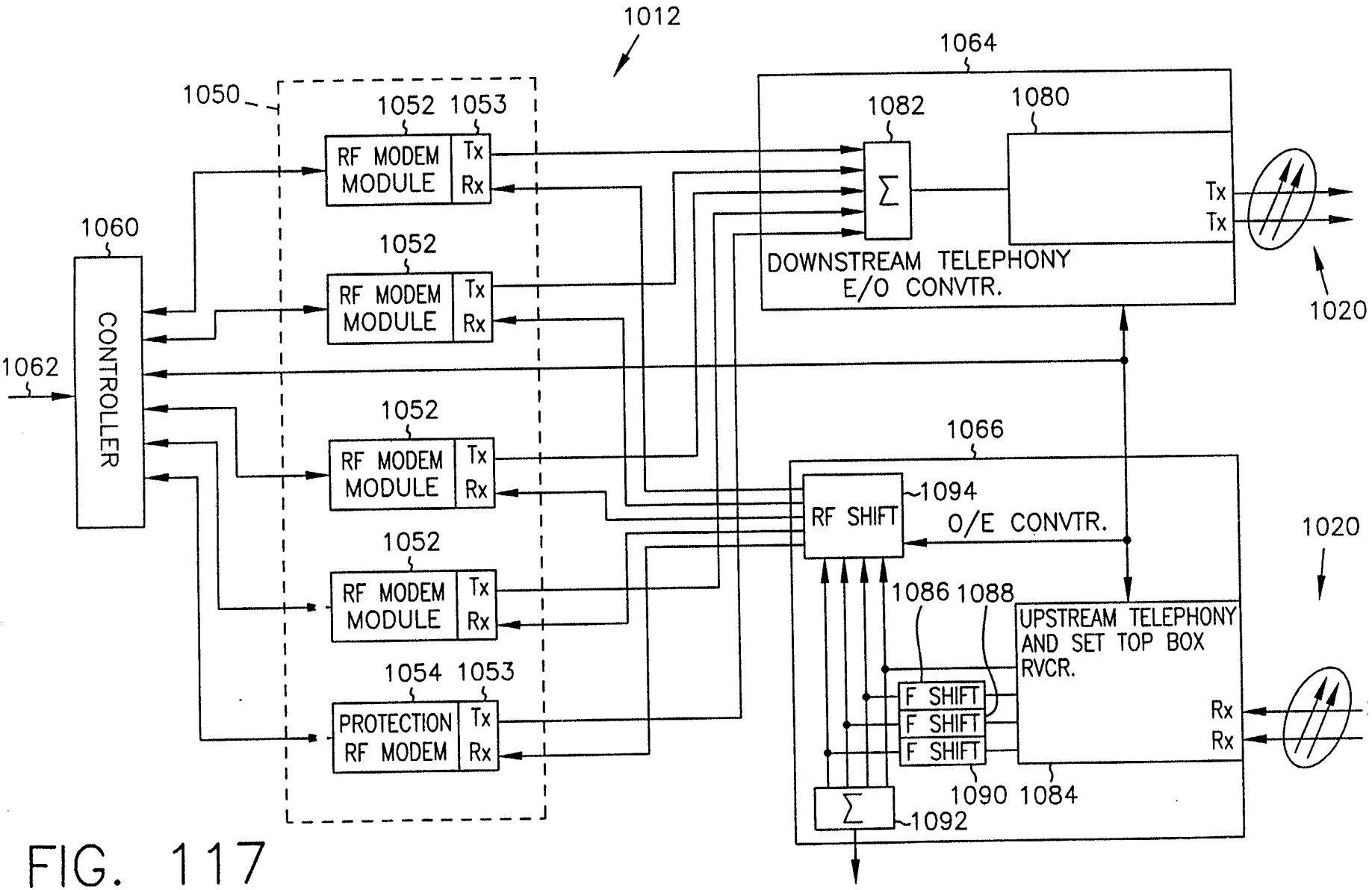

1012
1050
1052 1053
RF MODEM MODULE
Tx
Rx
1052
RF MODEM MODULE
1052
RF MODEM MODULE
1052
RF MODEM MODULE
1054 1053
PROTECTION RF MODEM
1060
CONTROLLER
1062
1064
1082
1080
Σ
DOWNSTREAM TELEPHONY E/O CONVTR.
Tx
Tx
1020
1066
RF SHIFT
1094
O/E CONVTR.
1020
1086 1088
UPSTREAM TELEPHONY AND SET TOP BOX RVCR.
F SHIFT
F SHIFT
F SHIFT
Rx
Rx
1090 1084
Σ
1092

FIG. 117

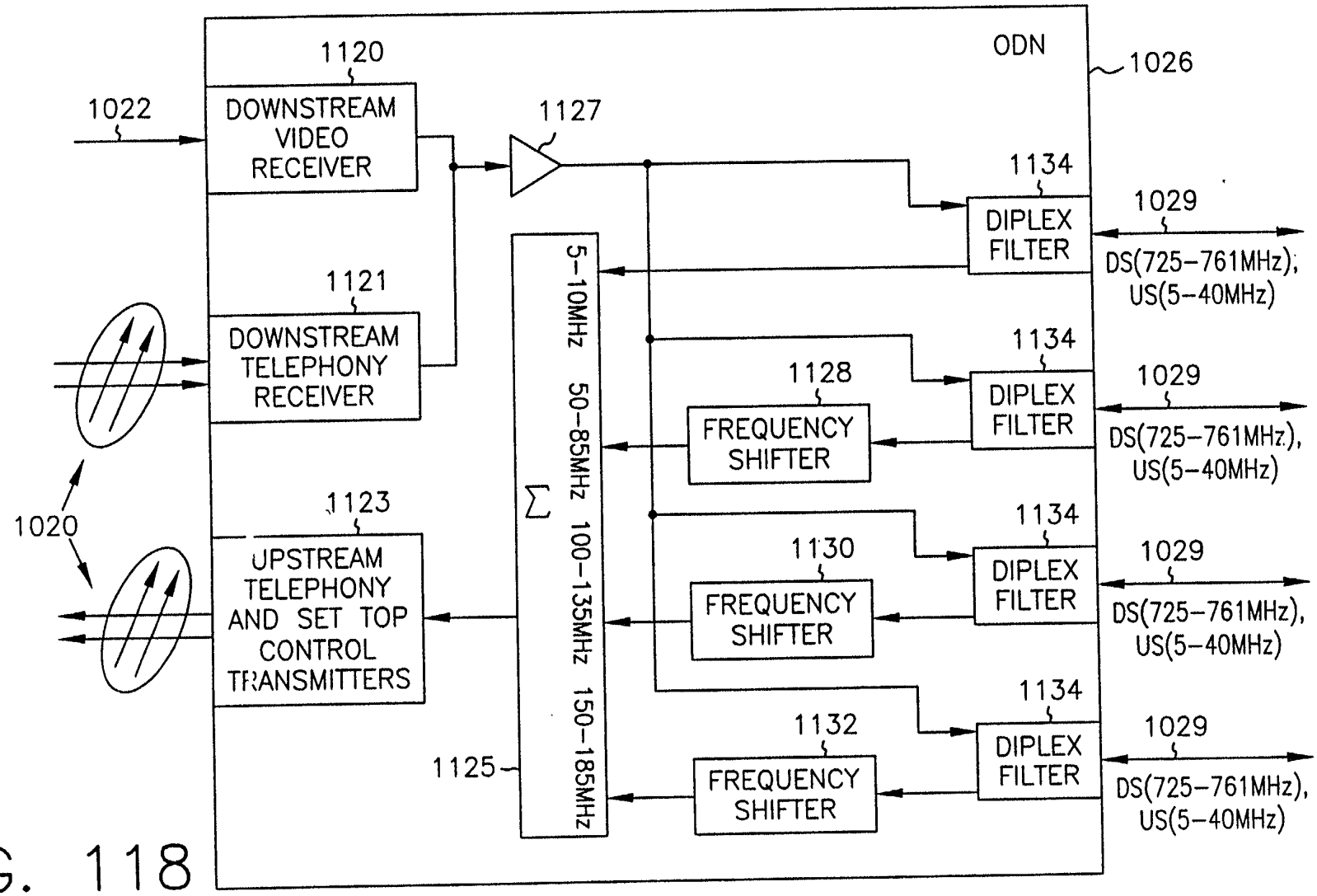

ODN
1026
1120
DOWNSTREAM VIDEO RECEIVER
1022
1127
1121
DOWNSTREAM TELEPHONY RECEIVER
1123
UPSTREAM TELEPHONY AND SET TOP CONTROL TRANSMITTERS
1020
1125
5–10MHz 50–85MHz 100–135MHz 150–185MHz
1128
FREQUENCY SHIFTER
1130
FREQUENCY SHIFTER
1132
FREQUENCY SHIFTER
1134
DIPLEX FILTER
1134
DIPLEX FILTER
1134
DIPLEX FILTER
1134
DIPLEX FILTER
1029
DS(725–761MHz), US(5–40MHz)
1029
DS(725–761MHz), US(5–40MHz)
1029
DS(725–761MHz), US(5–40MHz)
1029
DS(725–761MHz), US(5–40MHz)

FIG. 118

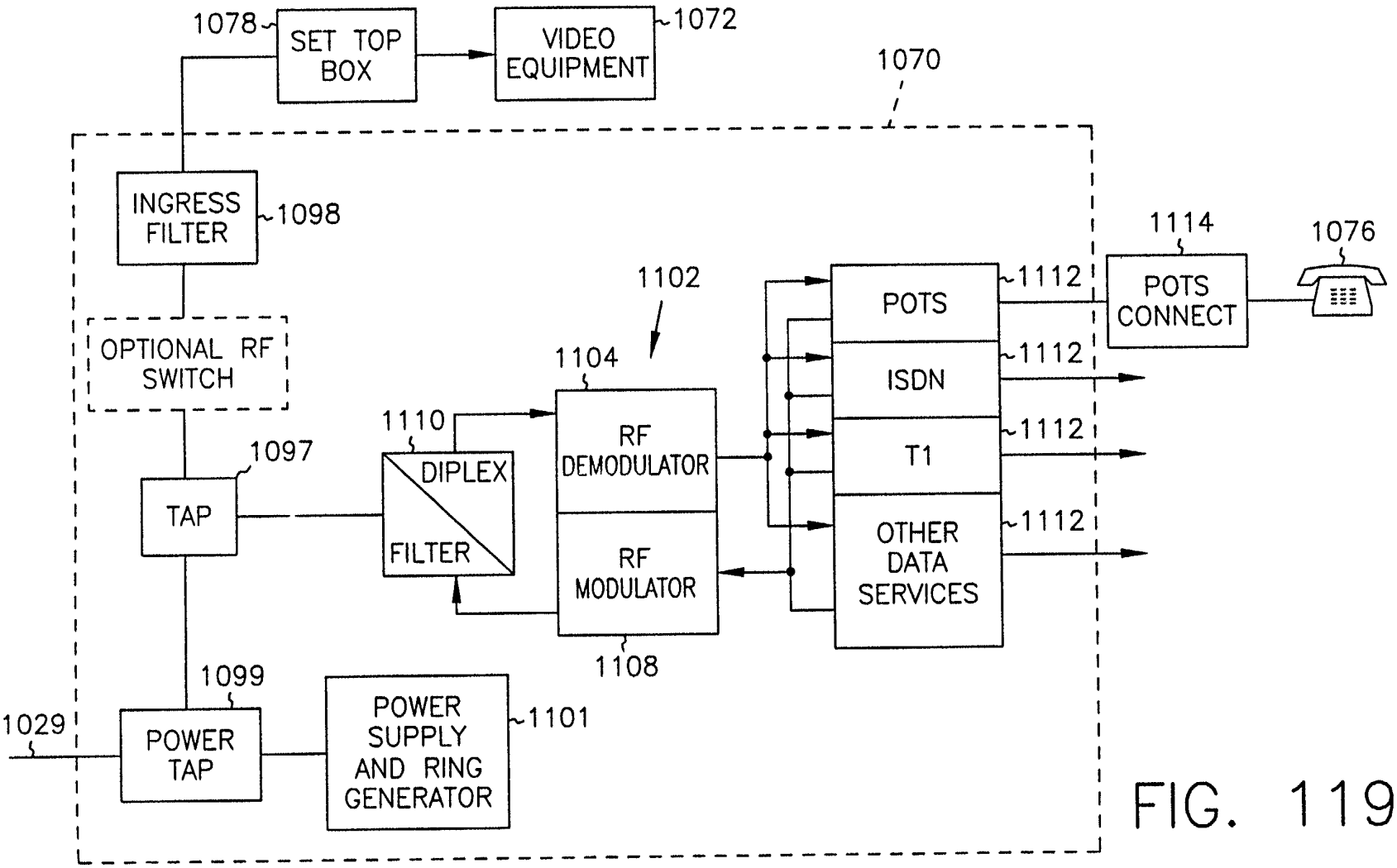

1078
SET TOP BOX
VIDEO EQUIPMENT
1072
1070
INGRESS FILTER
1098
OPTIONAL RF SWITCH
1097
TAP
1110
DIPLEX FILTER
1102
1104
RF DEMODULATOR
RF MODULATOR
1108
POTS
ISDN
T1
OTHER DATA SERVICES
1112
1114
POTS CONNECT
1076
1099
POWER TAP
1029
POWER SUPPLY AND RING GENERATOR
1101

FIG. 119

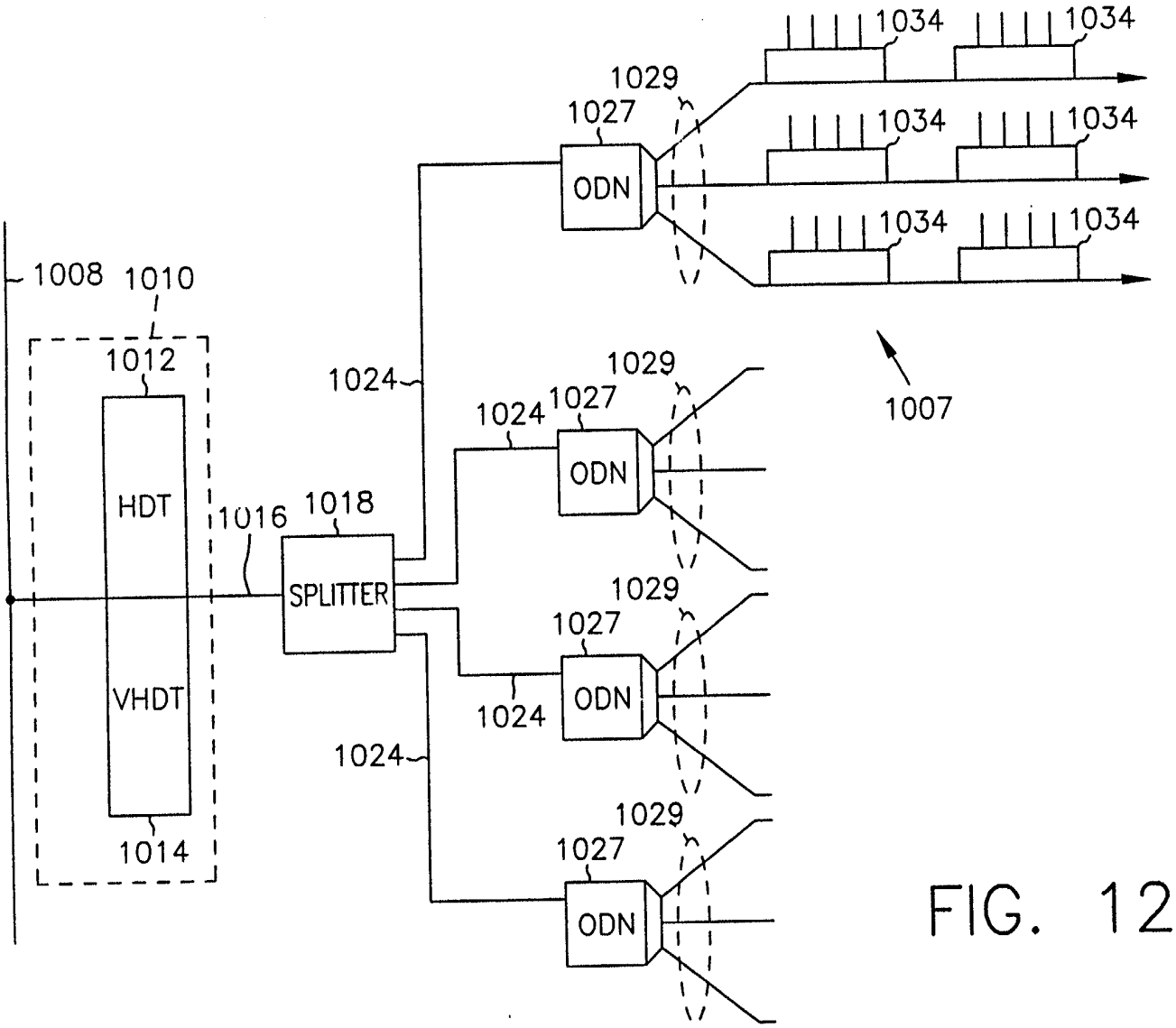

1008
1010
1012
HDT
VHDT
1014
1016
1018
SPLITTER
1024
1024
1024
1024
1027
1027
1027
1027
1029
1029
1029
1029
ODN
ODN
ODN
ODN
1034
1034
1034
1034
1034
1034
1007

FIG. 120

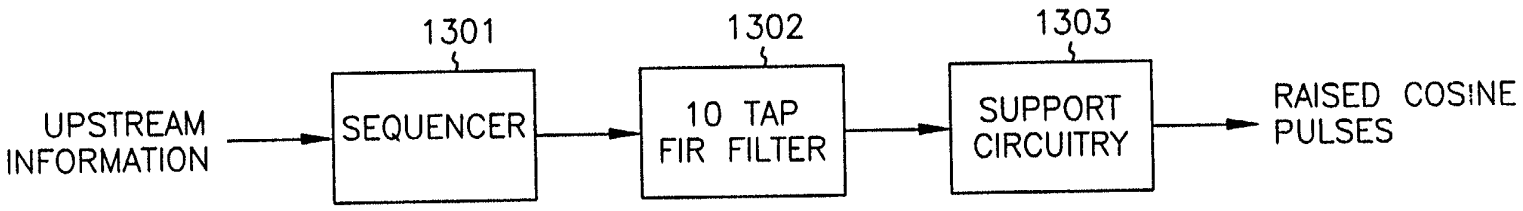


FIG. 121

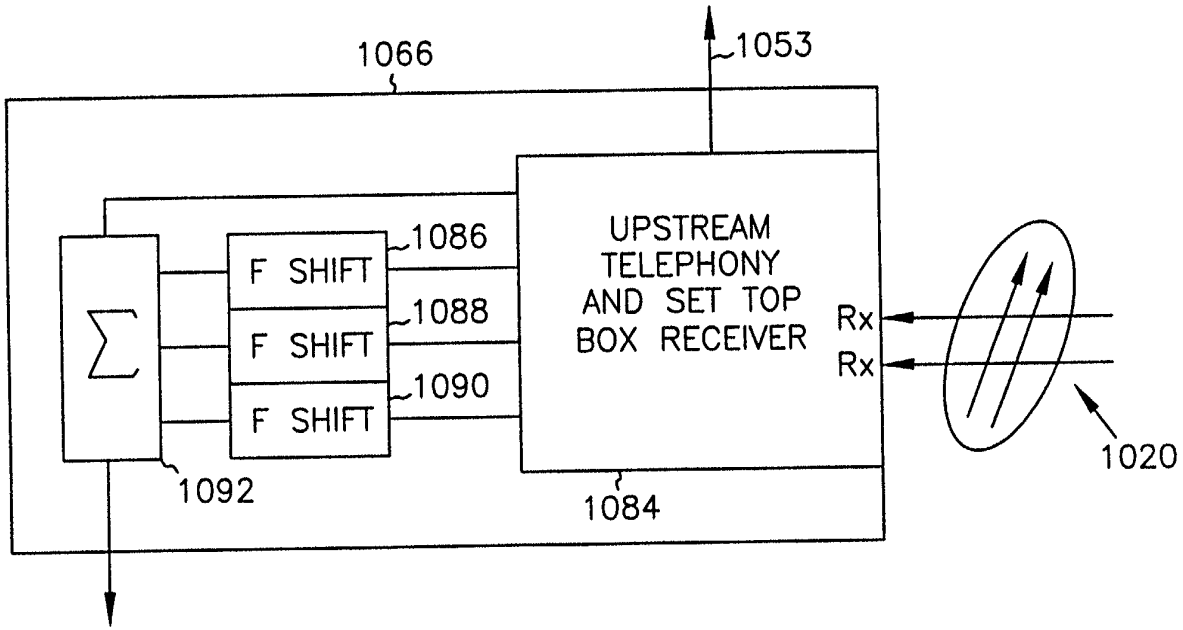

1066
1053
F SHIFT
1086
F SHIFT
1088
F SHIFT
1090
UPSTREAM TELEPHONY AND SET TOP BOX RECEIVER
Rx
Rx
1020
1092
1084

FIG. 122

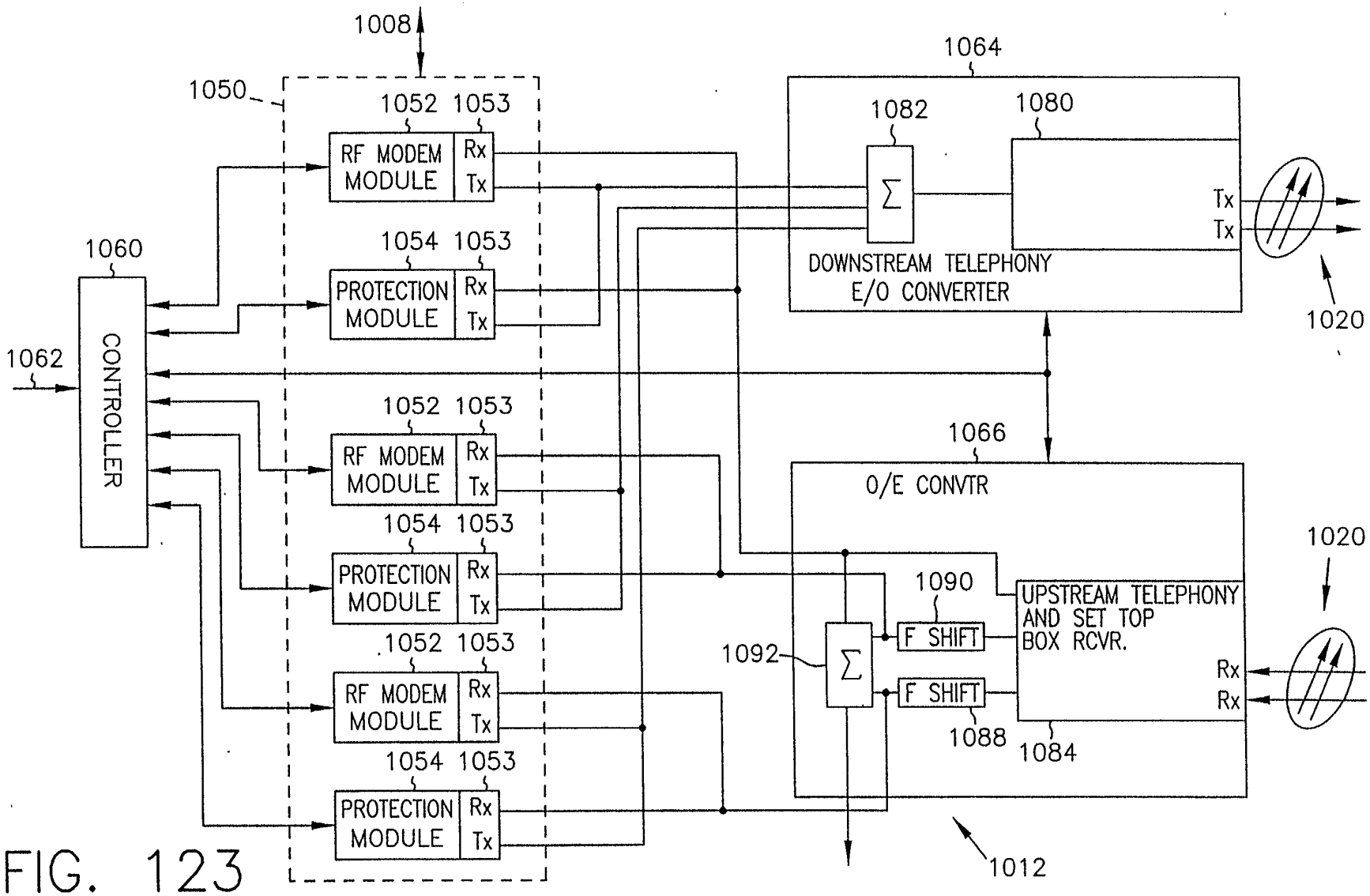

1008
1050
1052 1053
RF MODEM MODULE
Rx
Tx
1054 1053
PROTECTION MODULE
Rx
Tx
1060
1062
CONTROLLER
1064
1082
1080
Σ
Tx
Tx
DOWNSTREAM TELEPHONY E/O CONVERTER
1020
1066
O/E CONVTR
1090
F SHIFT
1092
UPSTREAM TELEPHONY AND SET TOP BOX RCVR.
Rx
Rx
1088
1084
1012

FIG. 123